

COMPAL CONFIDENTIAL

MODEL NAME : QALA0
PCB NO : LA-7761P (DAZ0LH00100)
BOM P/N : 4319EI31L01,4319EI31L02,4319EI31L03,4319EI31L04.
GPIO P/N: E4 VC GPIO map rev 1.1


Dalmore 15 UMA
Ivy Bridge + Panther POINT
2012-02-22
REV : 1.0 (A00)
@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
TPM	4319EI31L01(R3) 4319EI31L03(R1)	1@ 3@
DTP	4319EI31L02(R3) 4319EI31L04(R1)	2@ 3@

MB PCB	
Part Number	Description
DA60000S00	PCB 0LH LA-7761P REV0 M/B UMA

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Title

Cover Sheet

Size

Document Number

LA-7761P

Rev

1.0

Date

Wednesday, February 22, 2012

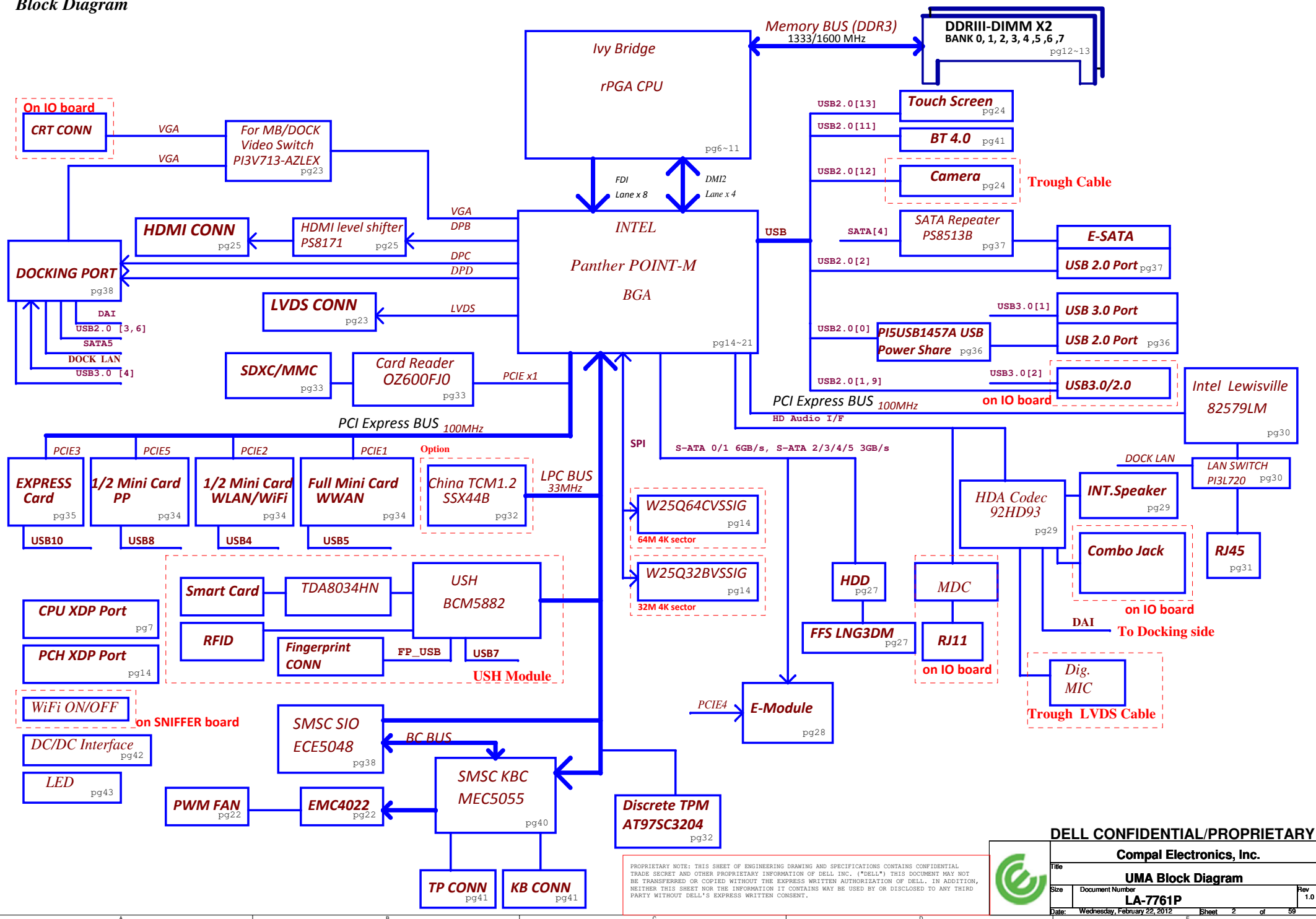
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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB 3.0 PORT#	Connetion
1	JUSB1 (Right side)
2	JUSB2 (Left side)
3	NA
4	DOCKING

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB2 (Left side)
	2	JESA1 (Right side ESATA)
	3	DOCKING
	4	WLAN
	5	WWAN
	6	DOCKING
	7	USH->BIO
	8	JMINI3(Flash)
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

Please get below information from Layout/Randy for PCB stack up.

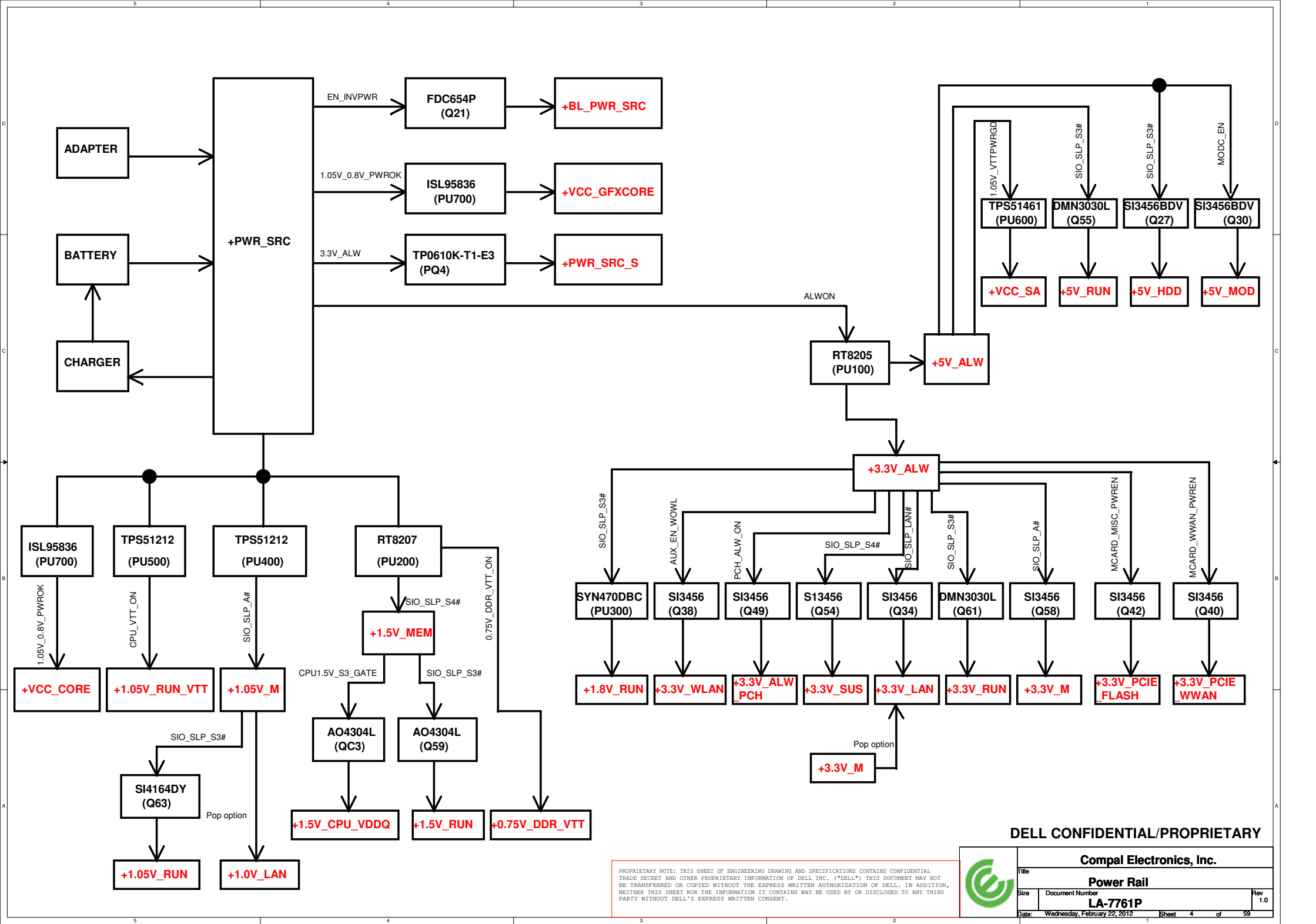
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask		0.50
			Add Plating		1.45
1	Top		Copper foil	0.5oz	0.65
			Prepreg	1080	2.60
2	VCC		Copper foil	1oz	1.35
			Core	3mil	3.00
3	Sig 1		Copper foil	1oz	1.35
			Prepreg	7628 HRC*2+2116+7628 HRC*2	33.50
4	Sig 2		Copper foil	1oz	1.35
			Core	3mil	3.00
5	GND		Copper foil	1oz	1.35
			Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.45
			SolderMask		0.50
Overall Thickness (1.4mm ± 10%)				55.1	55.30000
					1.40462

need to update Power Status and PM Table

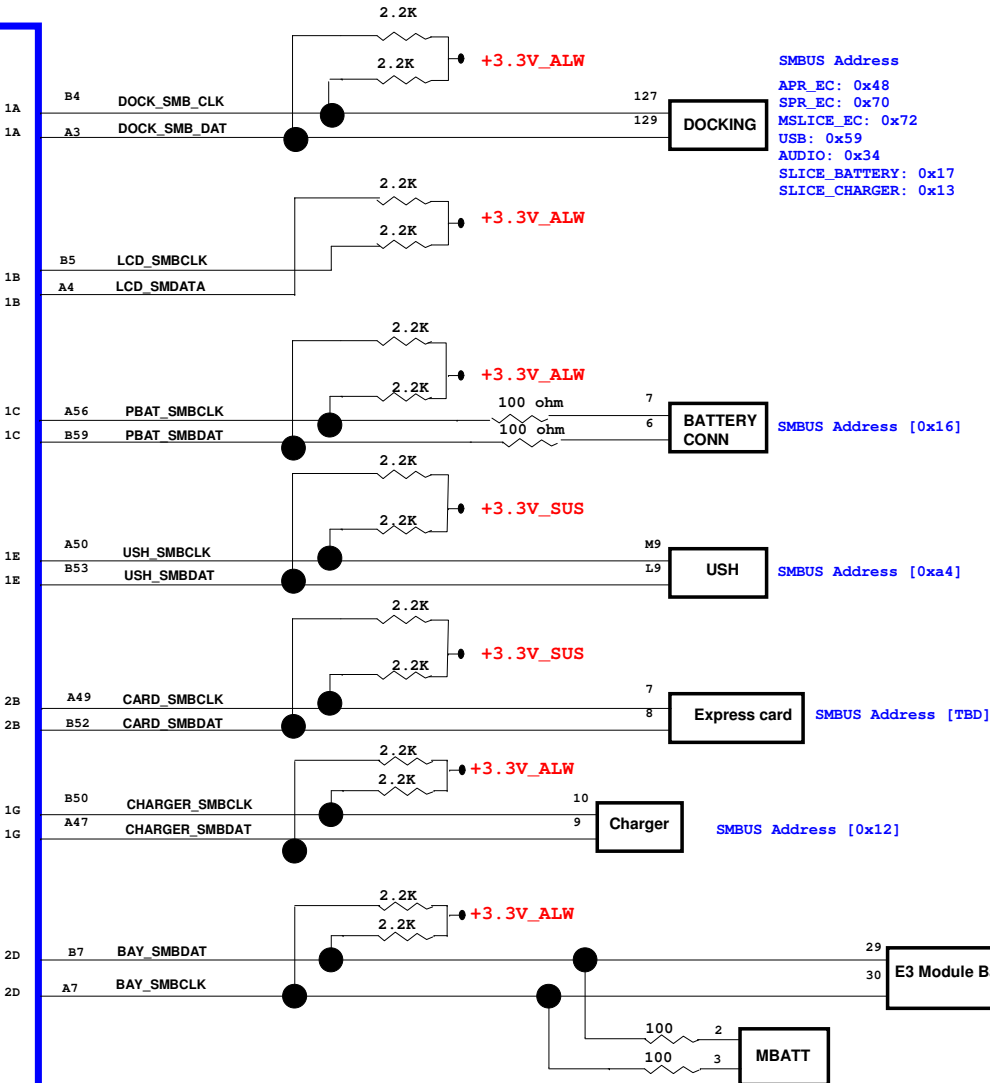
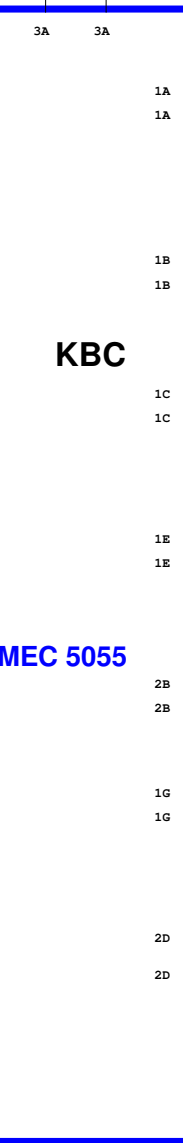
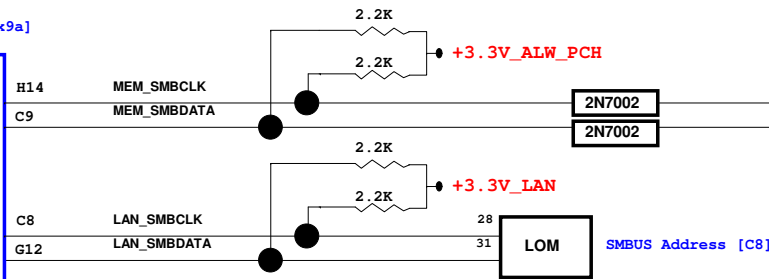
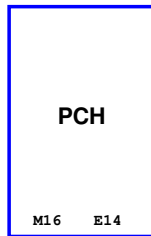
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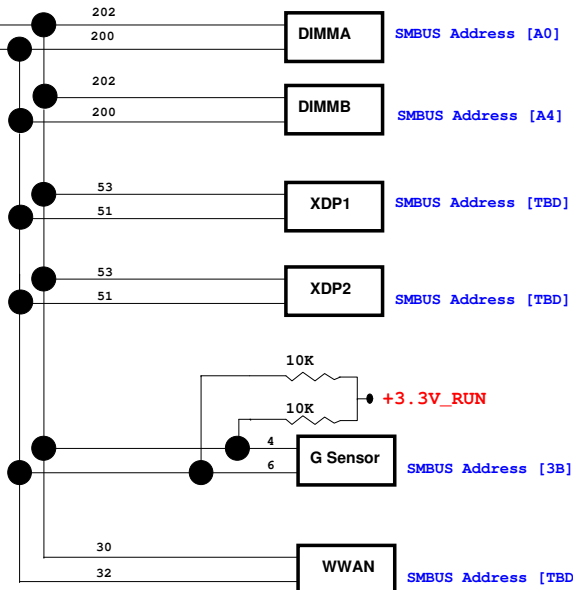
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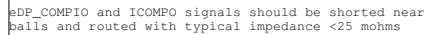
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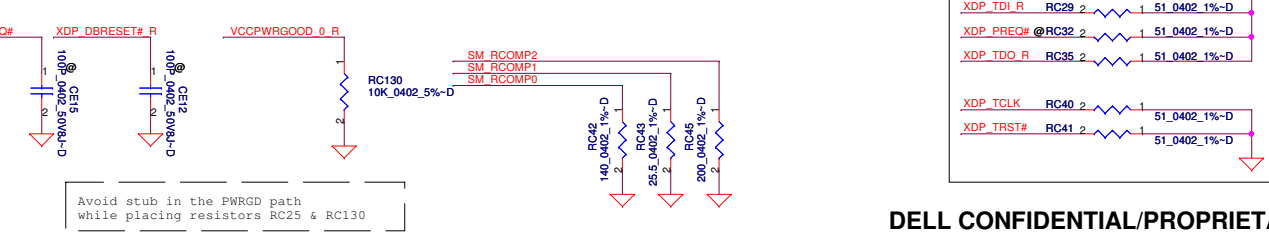
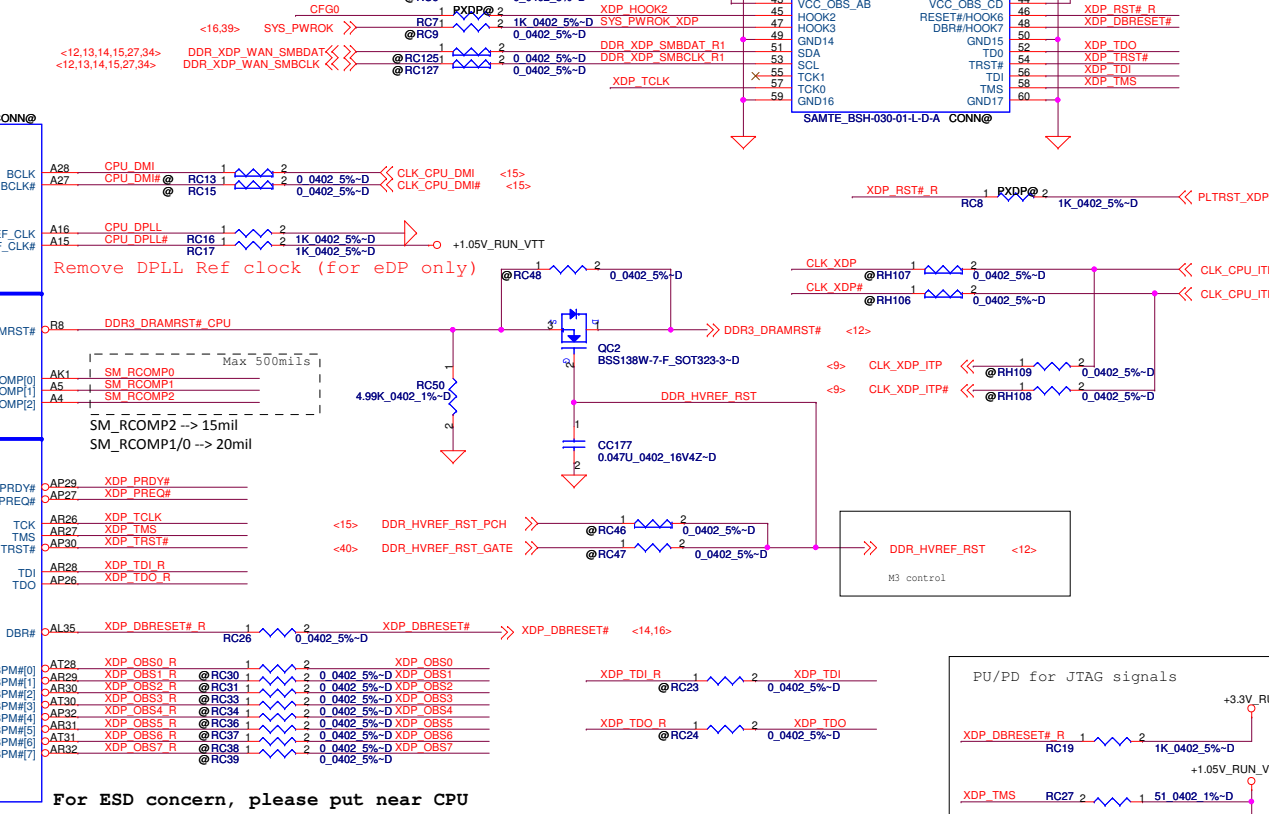
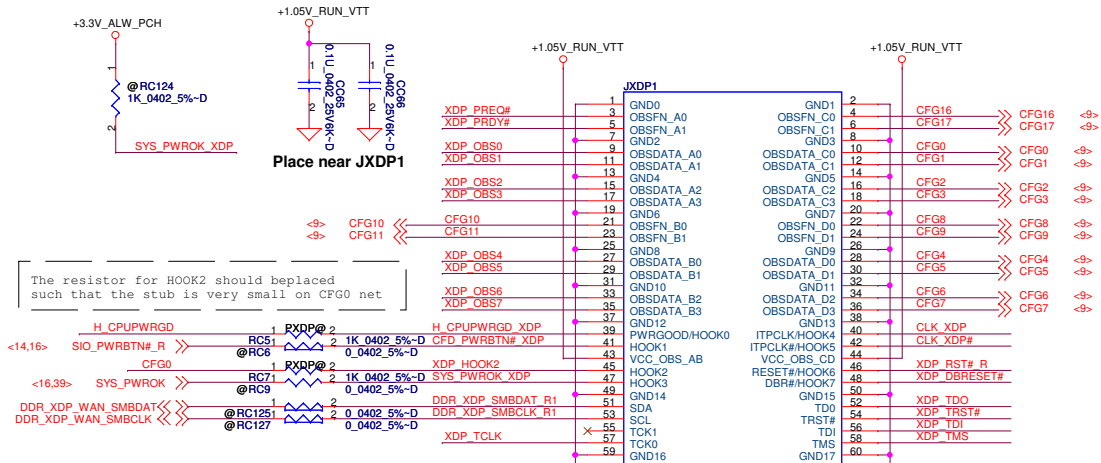
SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

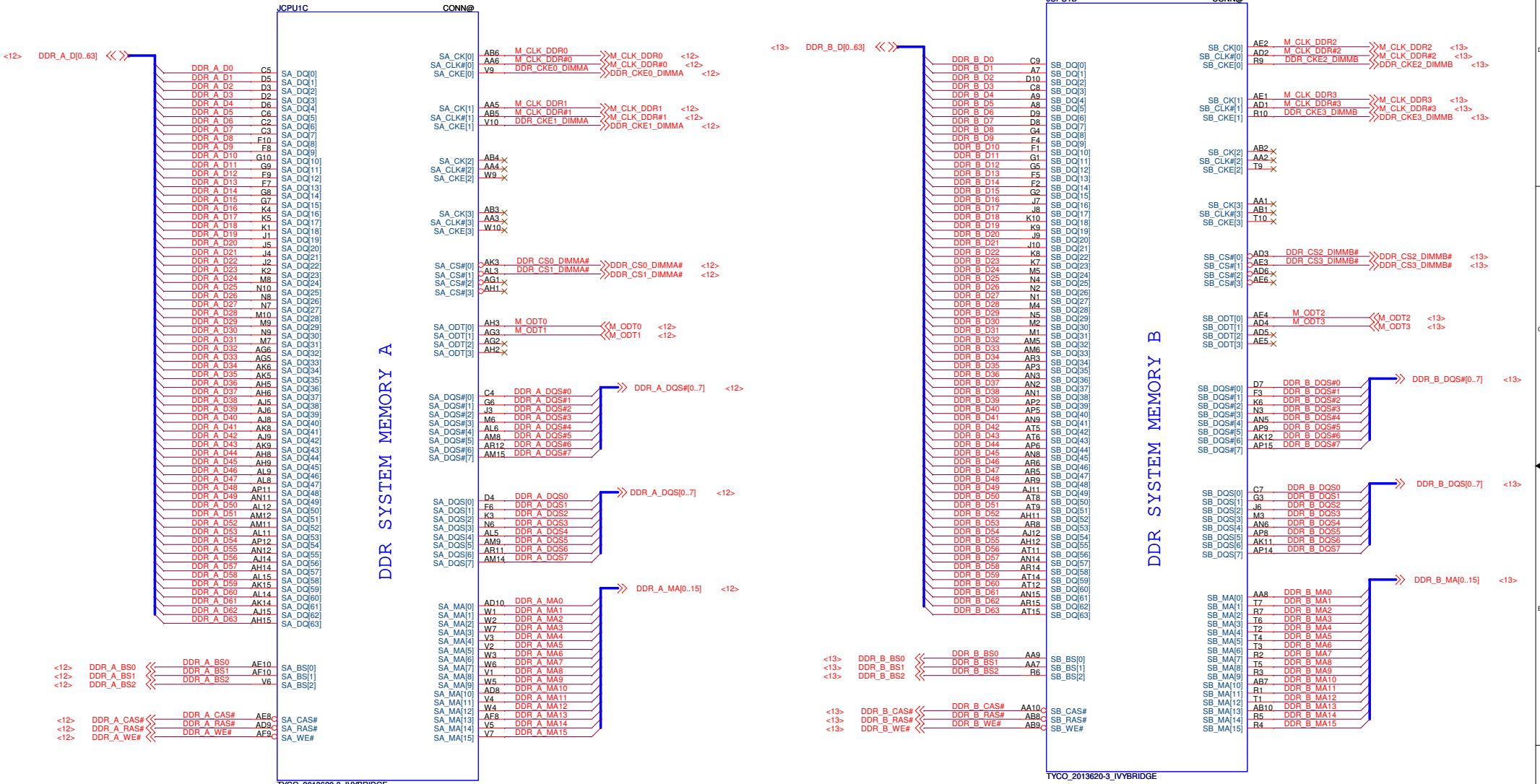


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A schematic diagram showing a resistor labeled RC56 (1K_0402_5%) connected between the CFG7 pin and ground. The pin is labeled 'CFG7' and the resistor is labeled '@RC56 1K_0402_5%'. The ground symbol is a triangle pointing down.



POWER

JCPU1F

+VCC_CORE
53A

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AD26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
Y25 VCC61
Y24 VCC62
Y23 VCC63
Y22 VCC64
Y21 VCC65
Y20 VCC66
Y19 VCC67
Y18 VCC68
Y17 VCC69
Y16 VCC70
Y15 VCC71
Y14 VCC72
Y13 VCC73
Y12 VCC74
Y11 VCC75
Y10 VCC76
Y09 VCC77
Y08 VCC78
Y07 VCC79
Y06 VCC80
Y05 VCC81
Y04 VCC82
Y03 VCC83
Y02 VCC84
Y01 VCC85
Y00 VCC86
R35 VCC87
R34 VCC88
R33 VCC89
R32 VCC90
R31 VCC91
R30 VCC92
R29 VCC93
R28 VCC94
R27 VCC95
R26 VCC96
R25 VCC97
R24 VCC98
R23 VCC99
R22 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

TYCO_2013620-3_IVYBRIDGE

CONN@

+1.05V_RUN_VTT

8.5A

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AC10
VCCIO4 Y10
VCCIO5 U10
VCCIO6 P10
VCCIO7 L10
VCCIO8 J14
VCCIO9 J13
VCCIO10 J12
VCCIO11 J11
VCCIO12 H11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C13
VCCIO31 C12
VCCIO32 C14
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

H_CPU_SVIDALRT# 1 RC61 2 43_0402_5%-D <<VIDALERT_N <51>

+1.05V_RUN_VTT

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

H_CPU_SVIDALRT# <<<VIDSCLK <51> <<<VIDSOUT <51>

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

VIDSCLK 100_0402_50%~D CE13

VIDSOUT 100_0402_50%~D CE14

Place RC66, RC70 near CPU

@RC75 100_0402_1%-D

+VCC_CORE

RC66 100_0402_1%-D

VCCSENSE <51> VSSSENSE <51>

RC70 100_0402_1%-D

VCC_SENSE R A135 VCCSENSE R

VSS_SENSE R A134 VSSSENSE R

VCCIO_SENSE R B10 VTT_SENSE

VSS_SENSE_VCCIO R A10 VSSIO_SENSE R

RC68 10_0402_1%-D

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Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *
* Description		
5A to Mem controller(+1.5V_CPU_VDDQ)		
5-6A to 2 DIMMs/channel		
2-5A to +1.5V_RUN & +0.75V_DDR_VTT		

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Sandy Bridge (5/6)

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+1.5V_CPU_VDDQ Source

POWER

GRAPHICS

SA RAIL

MISC

JCPU1H

CONN@

JCPU1G

CONN@

VSS

TYCO_2013620-3_IVYBRIDGE

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Sandy Bridge (6/6)

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+1.5V_CPU_VDDQ Source

POWER

GRAPHICS

SA RAIL

MISC

JCPU1H

CONN@

JCPU1G

CONN@

VSS

TYCO_2013620-3_IVYBRIDGE

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Sandy Bridge (6/6)

LA-7761P

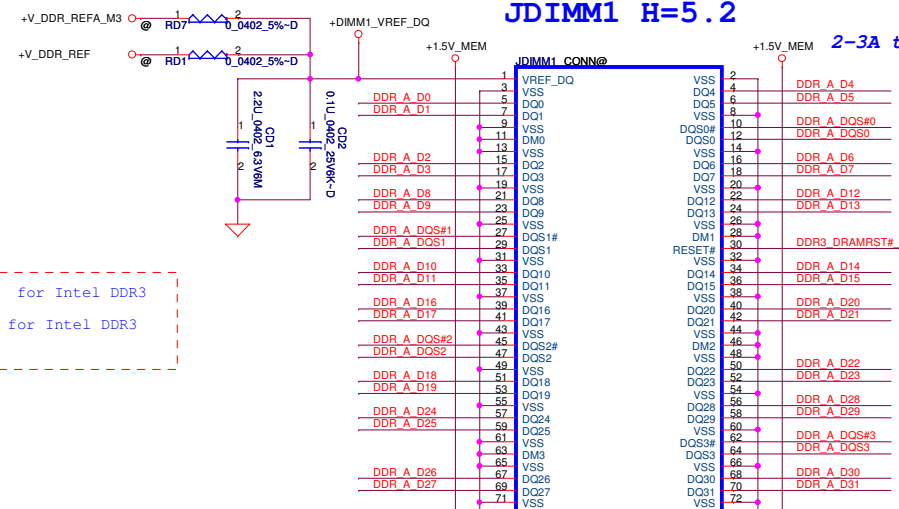
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JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

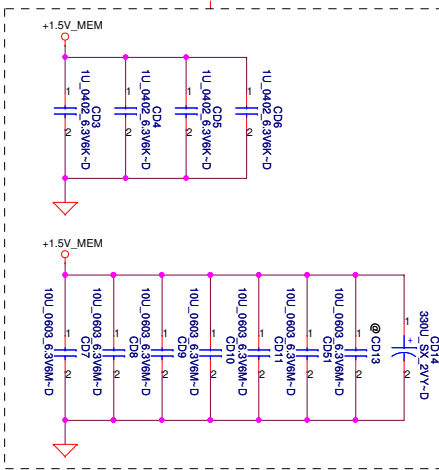


```
Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3
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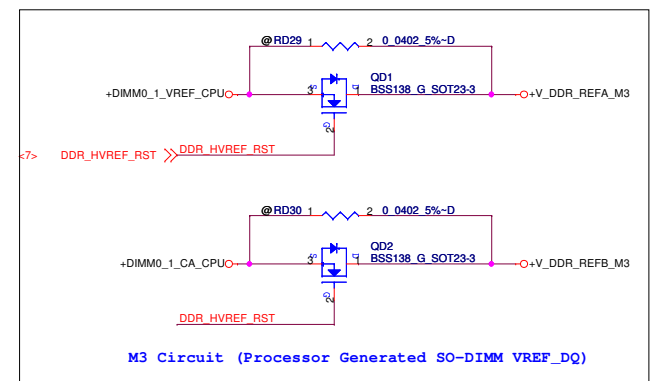
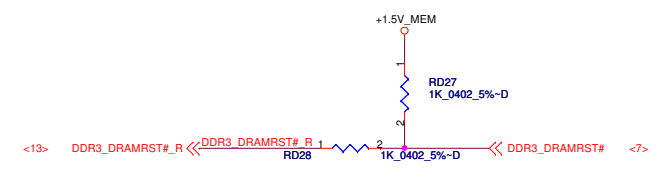
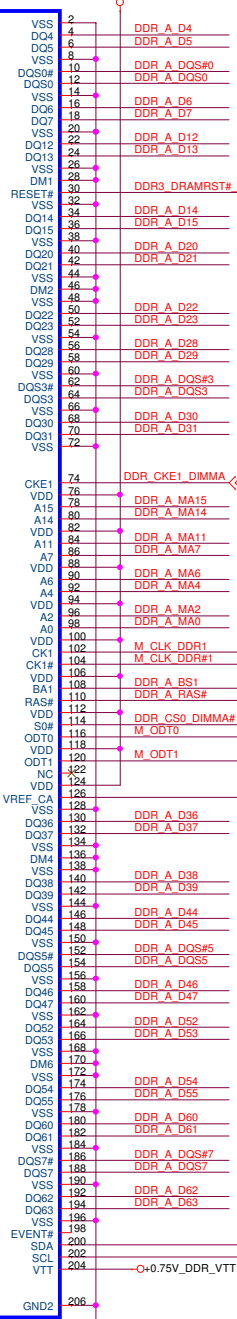
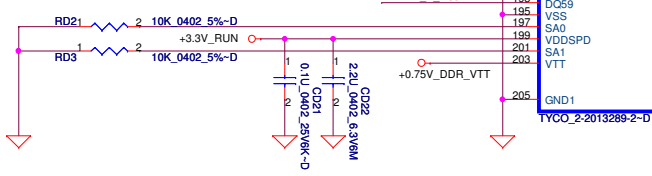
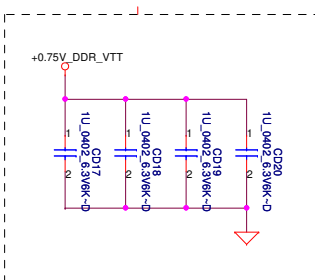
All VREF traces should have 10 mil trace width

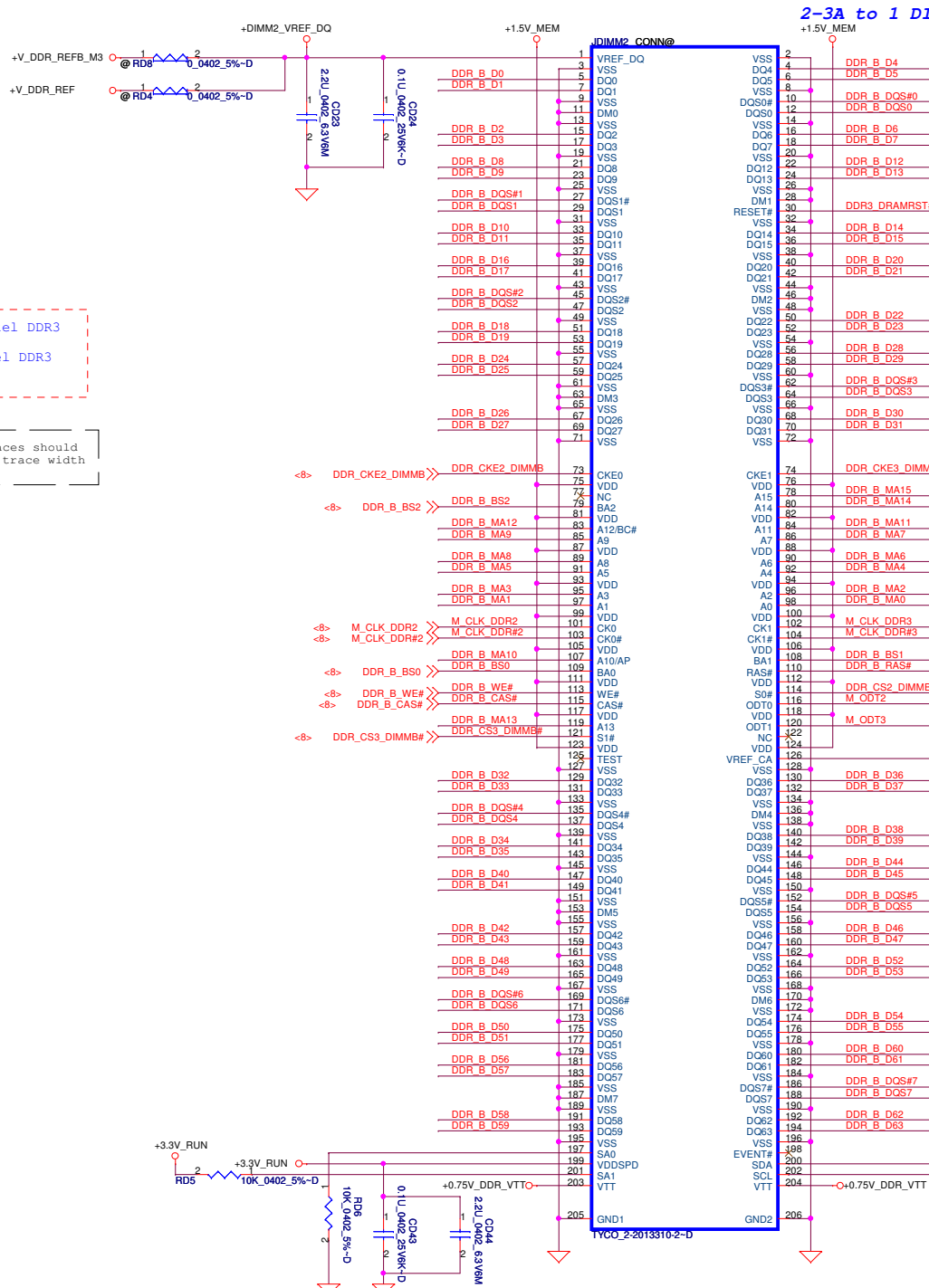


Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



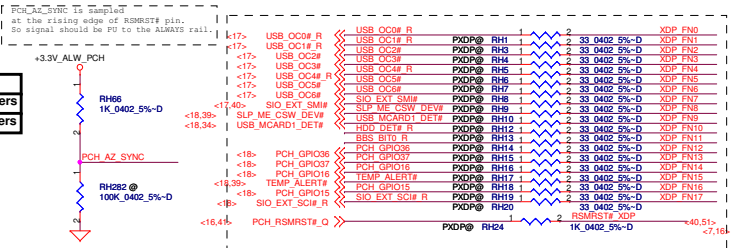
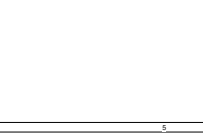
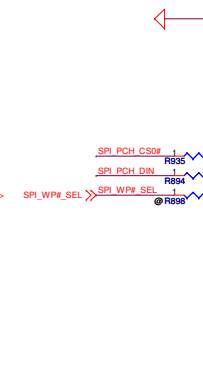
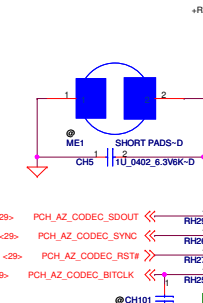
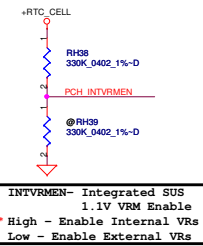


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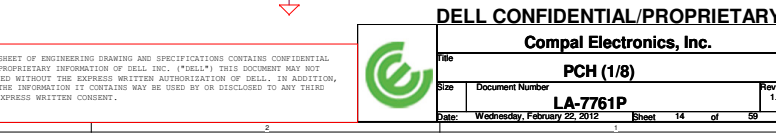
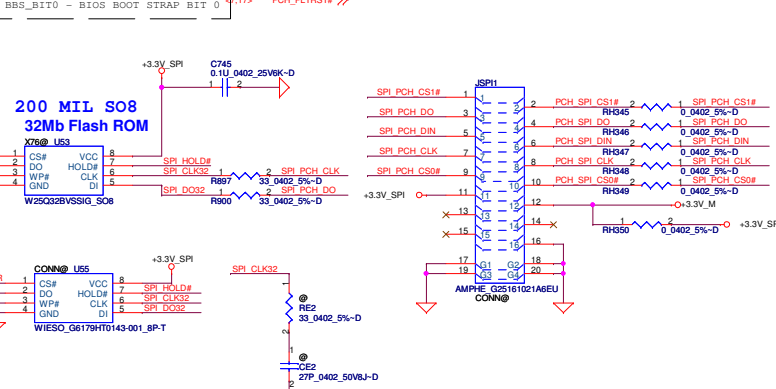
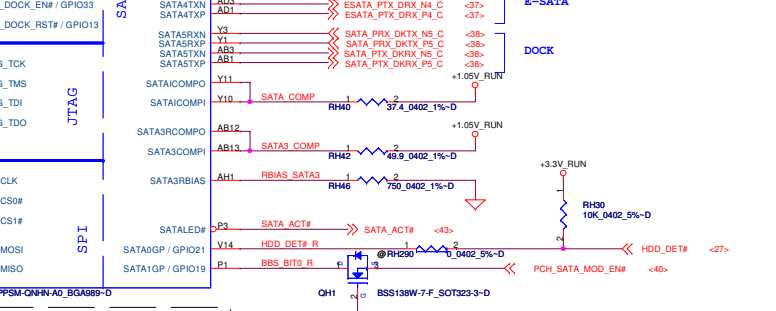
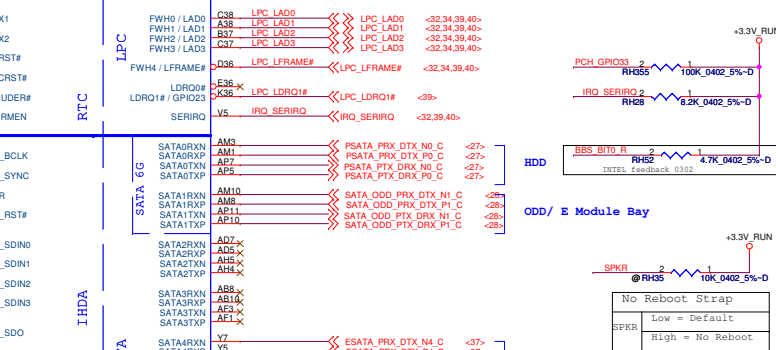
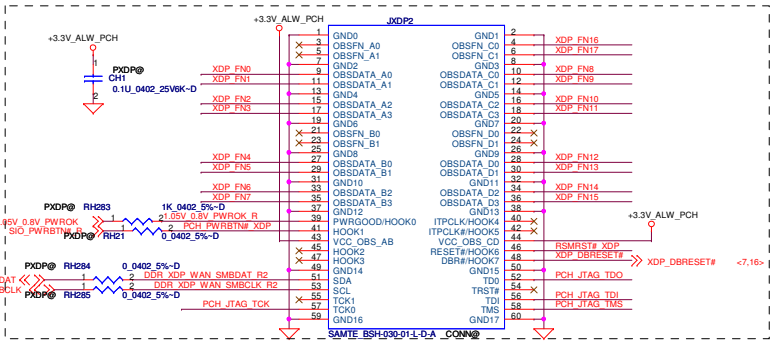
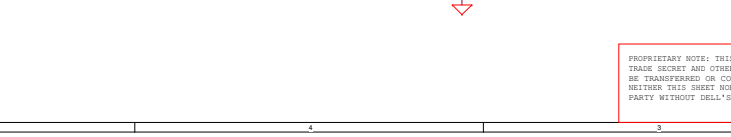
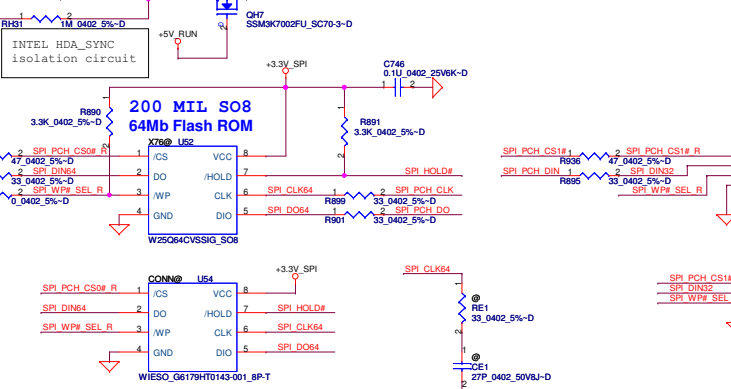
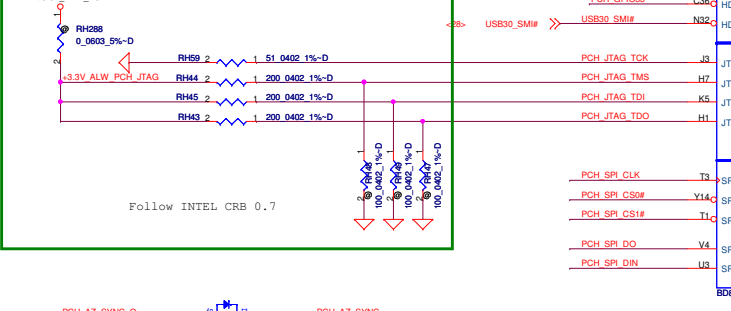
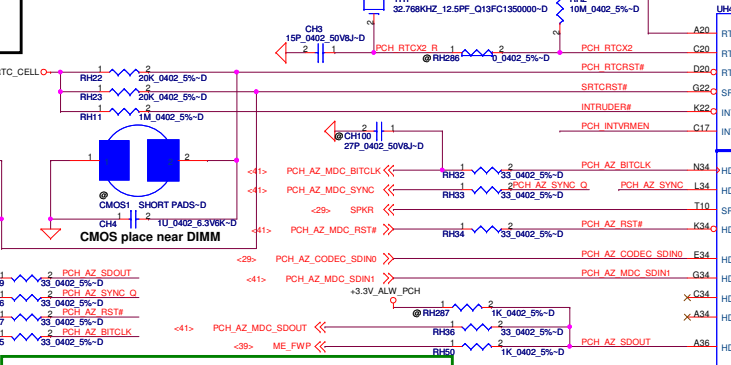


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DDR3II-SODIMM SLOT2			
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CMOS CLR1		CMOS setting	
Shunt	Clear CMOS	Open	Keep CMOS
ME CLR1		TPM setting	
Shunt	Clear ME RTC Registers	Open	Keep ME RTC Registers

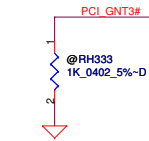
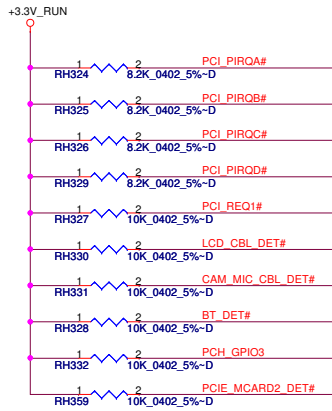


On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

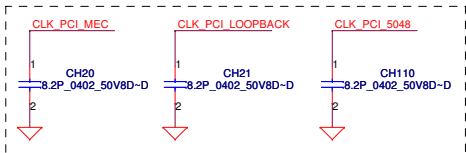
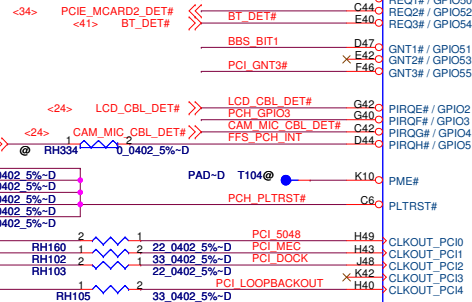


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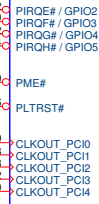
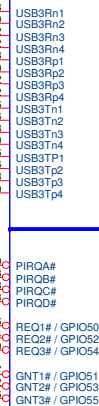
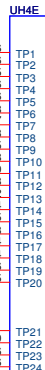
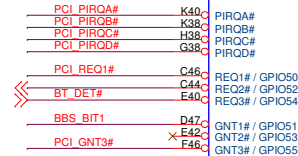
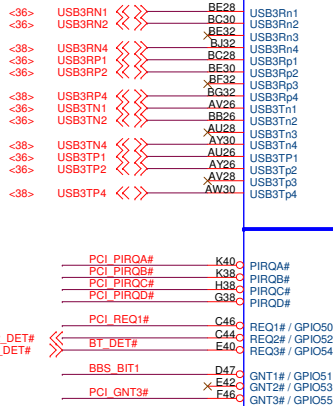
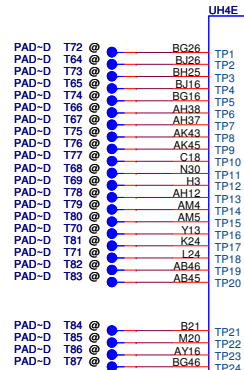
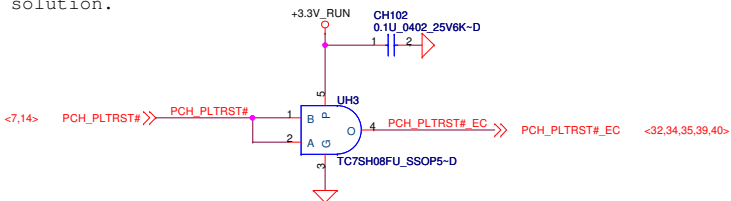




A16 swap override Strap/Top-Block	
Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

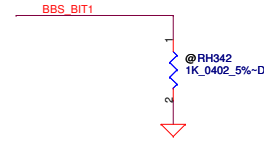


For RF noise solution.



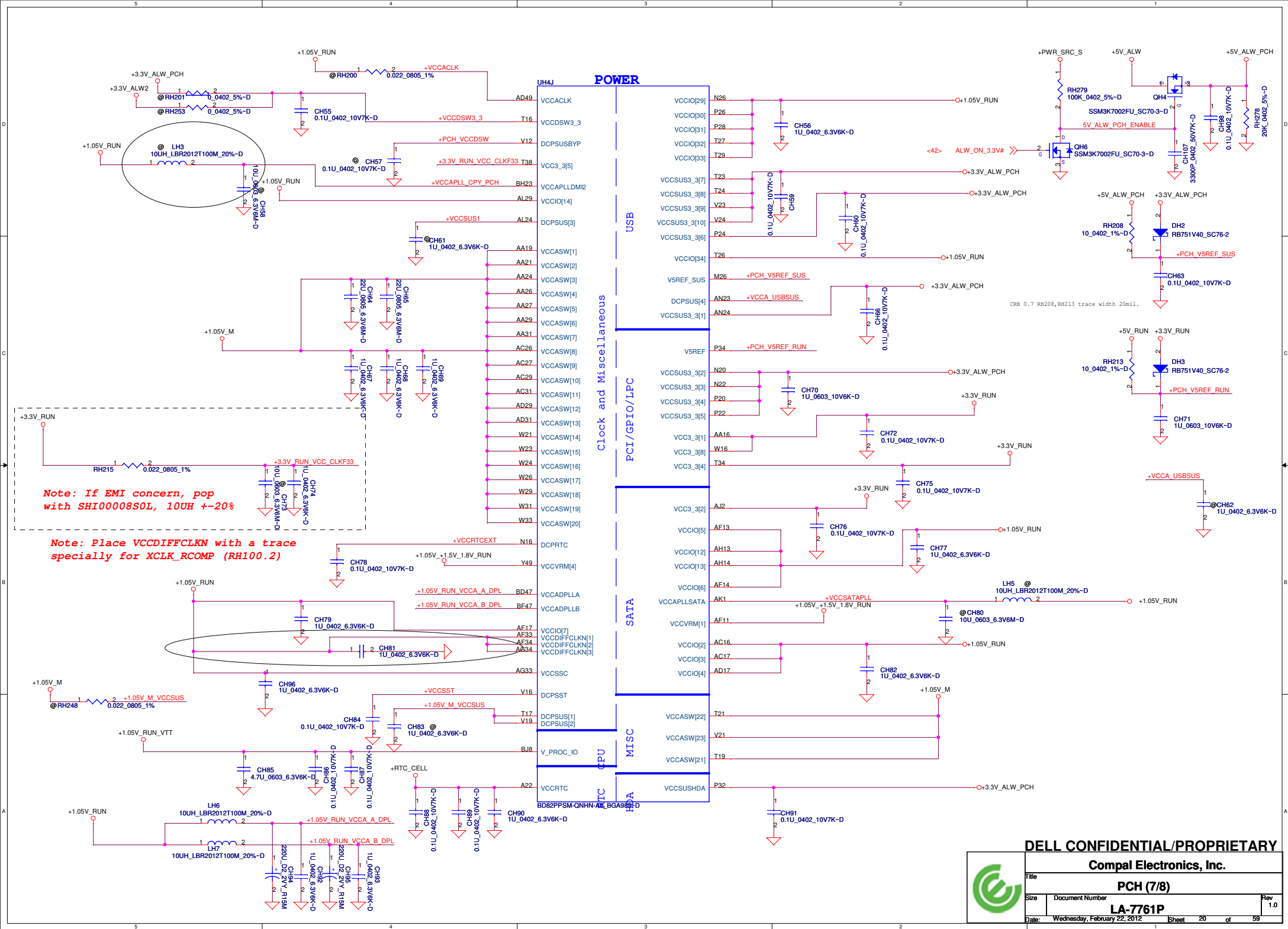
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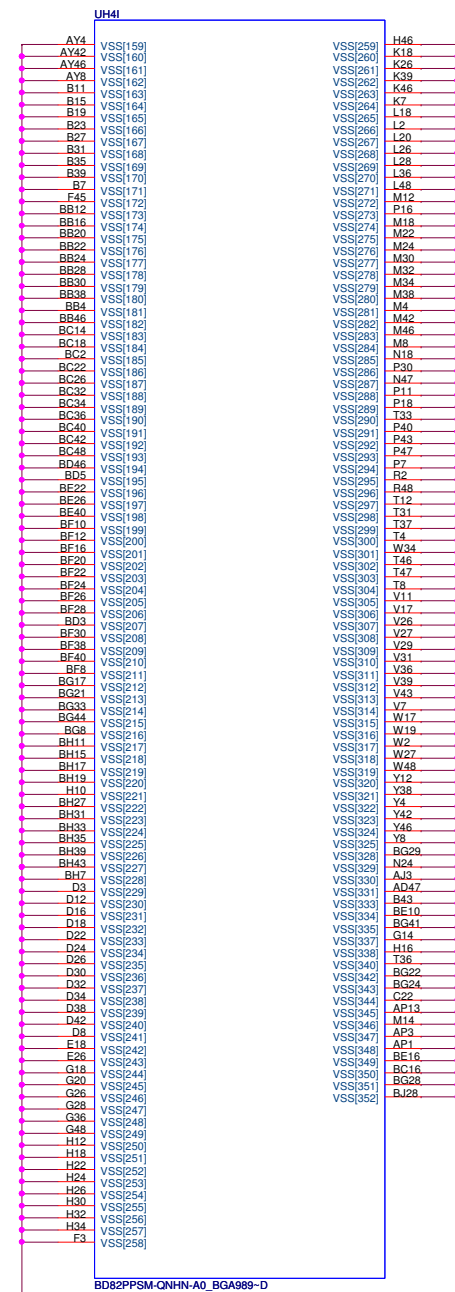
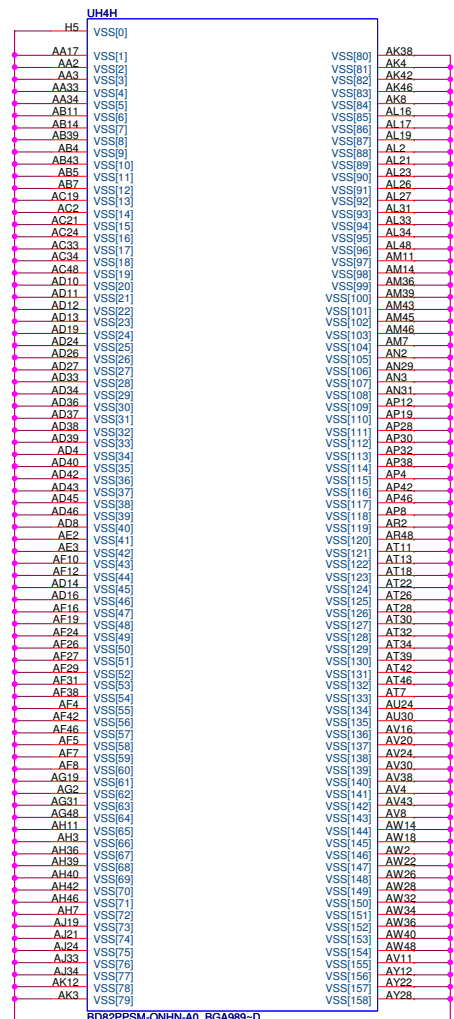
Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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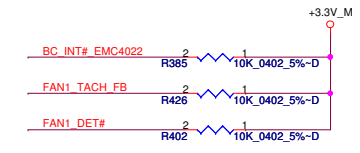
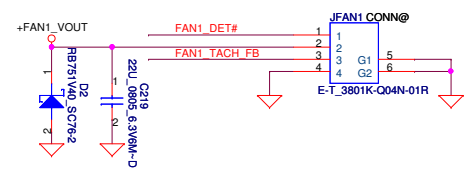
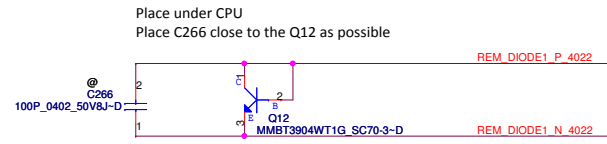


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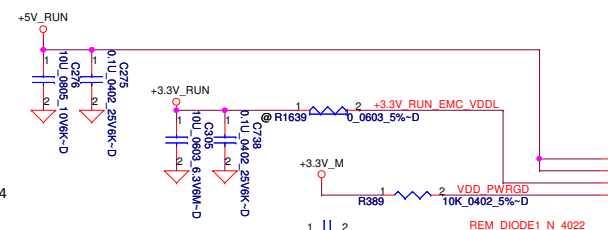
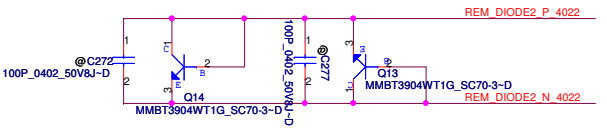
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Title	PCH (8/8)
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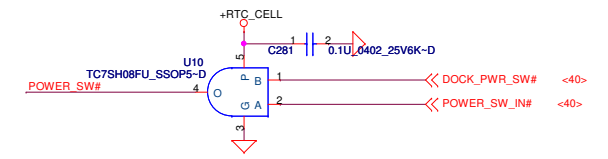
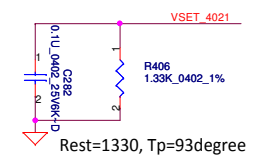
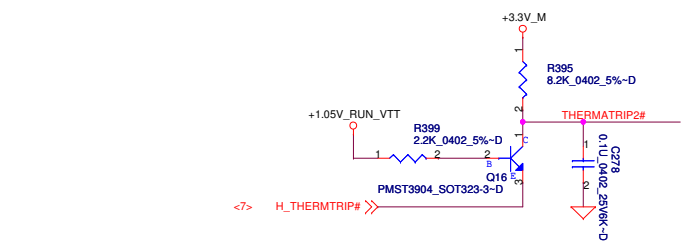
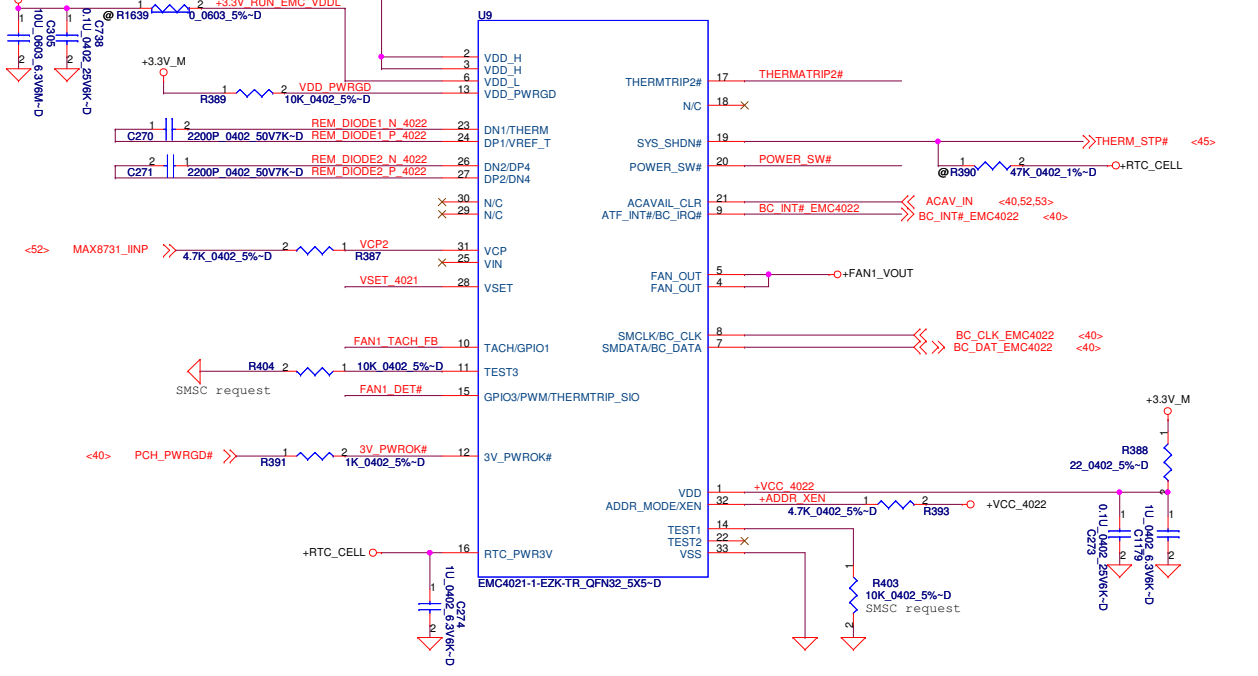
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- (1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.



Change to EMC4021 for cost saving

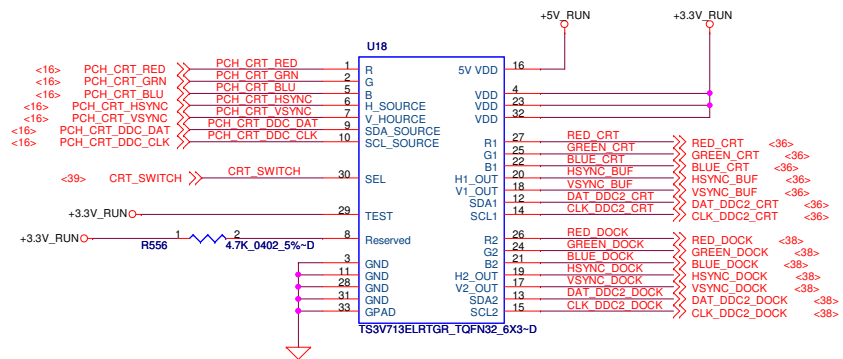


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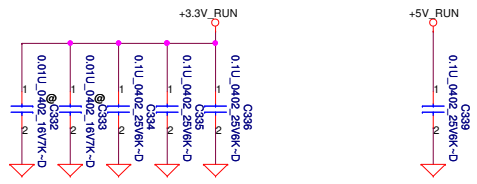
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Title			
FAN & Thermal Sensor			
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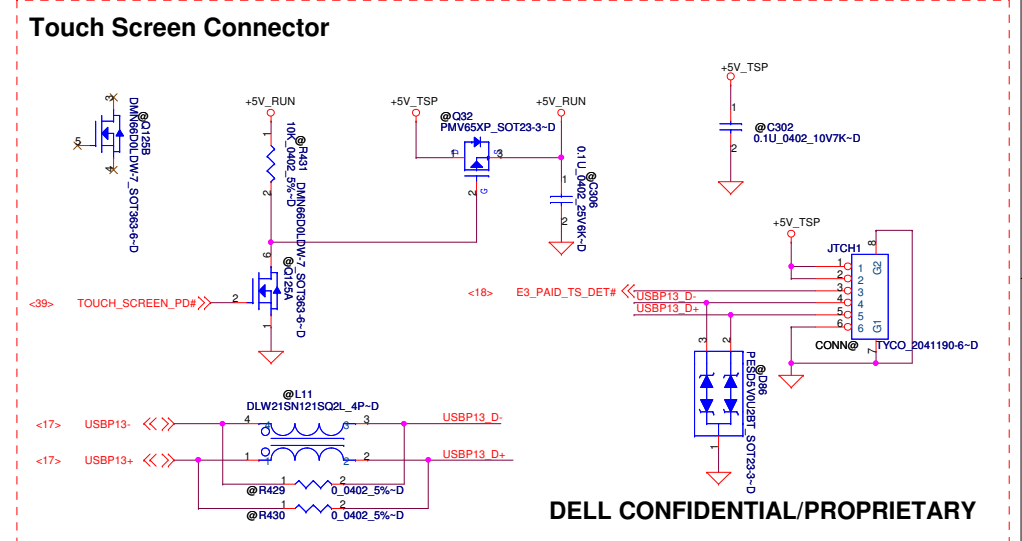
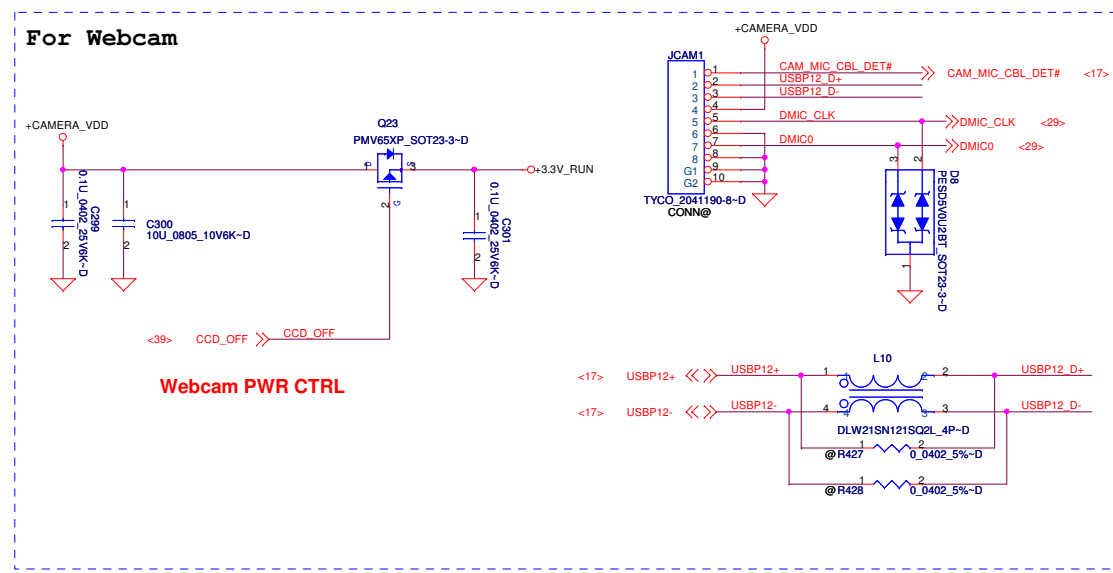
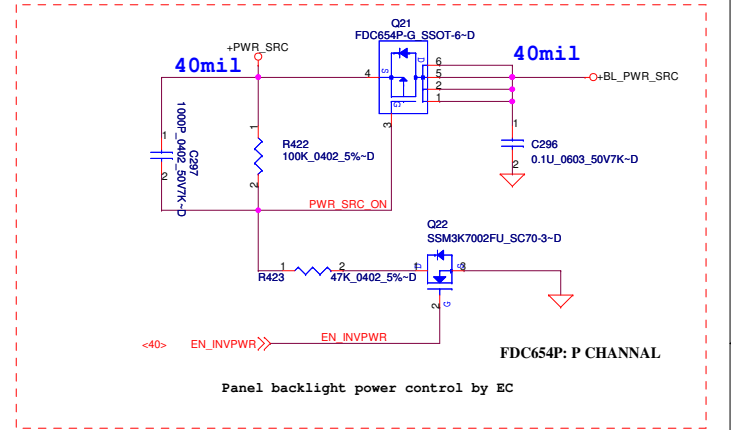
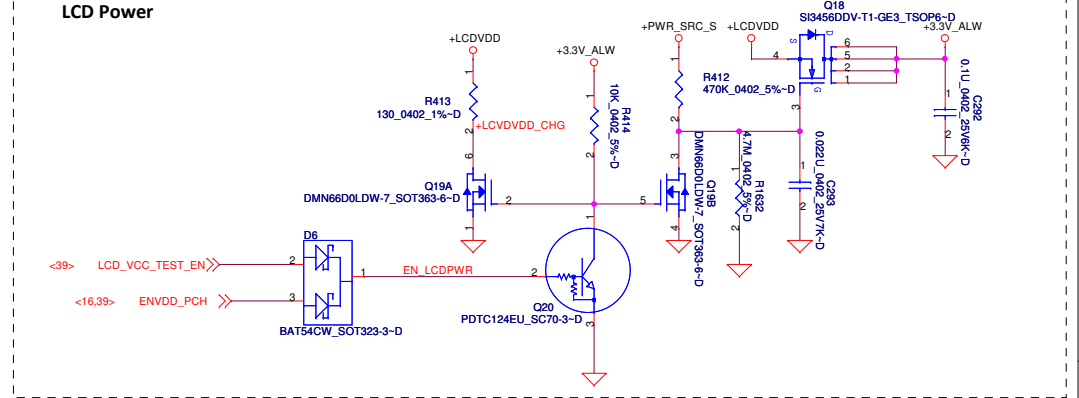
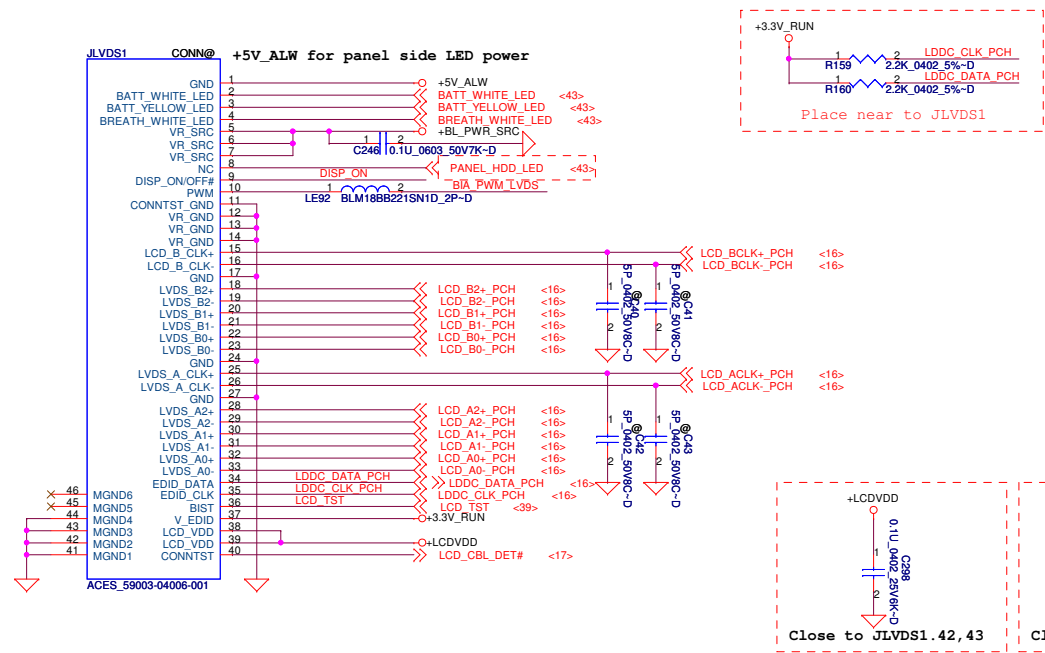
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SW for MB/DOCK



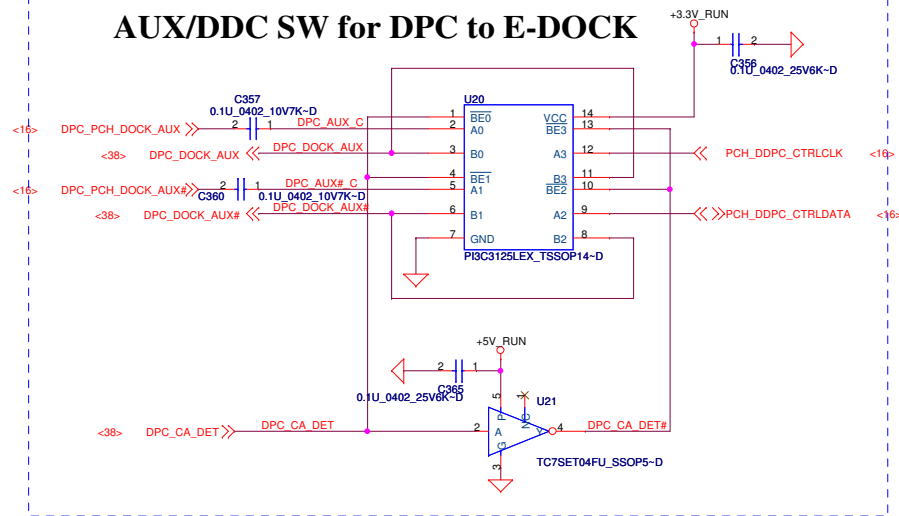
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR





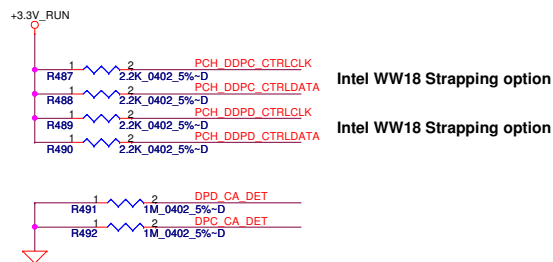
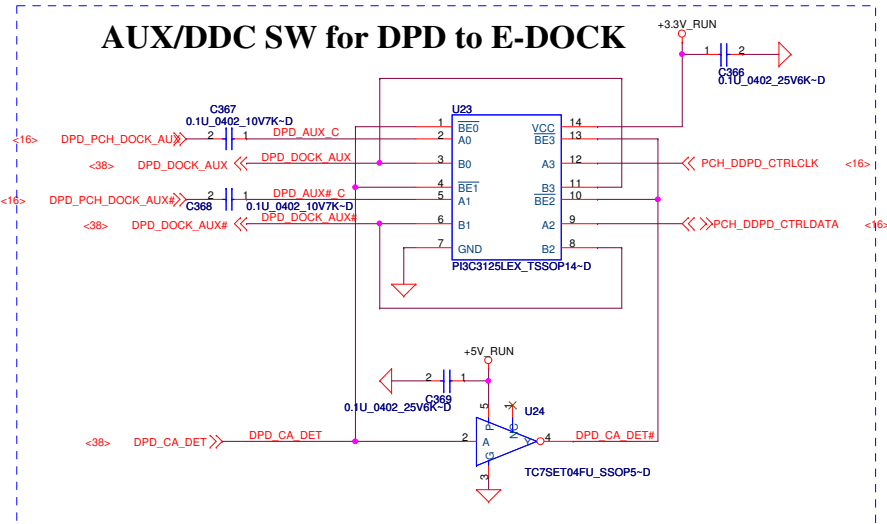
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AUX/DDC SW for DPC to E-DOCK




There is a new die for PI3C3125. Sample available on May.

AUX/DDC SW for DPD to E-DOCK



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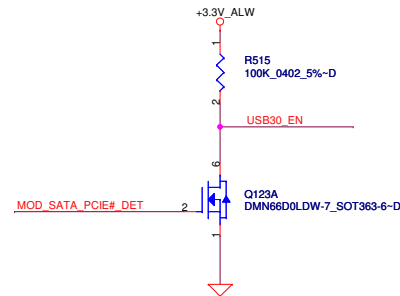
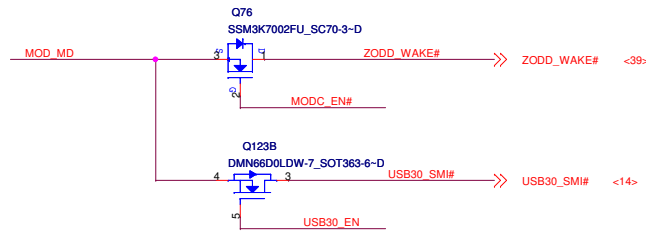
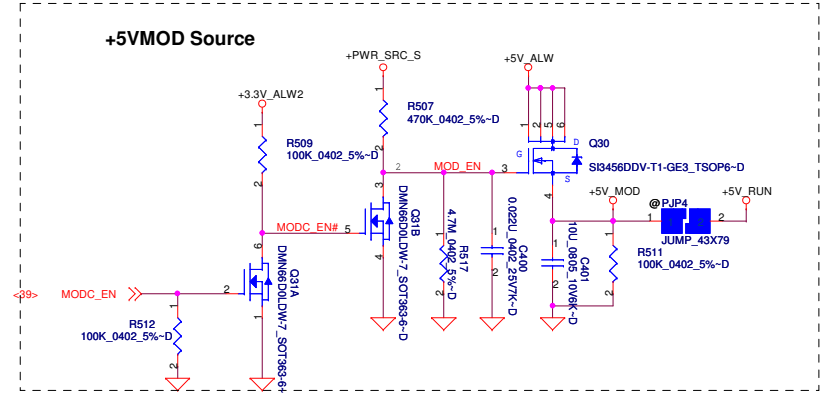
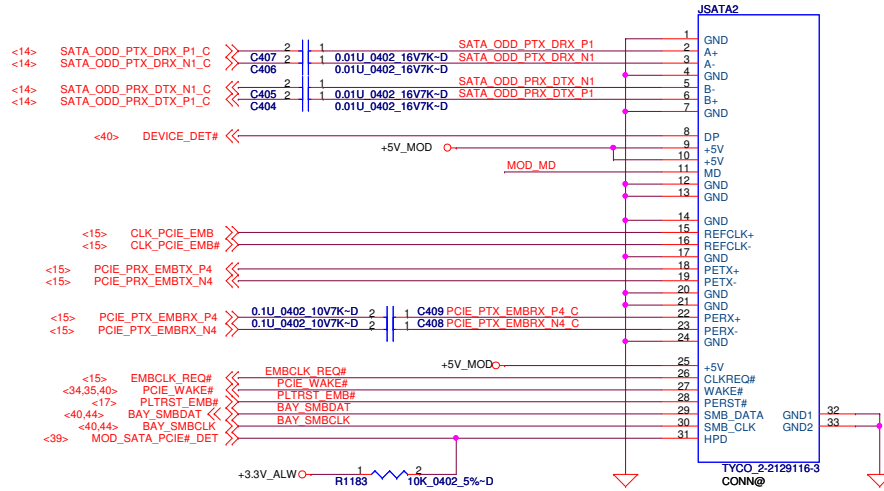
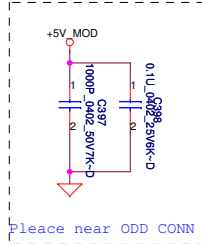
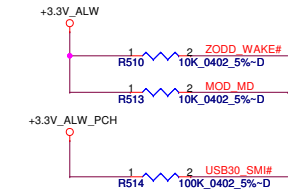
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+5V_HDD Source

For ODD



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15 mils trace

DVDD_IO should match with HDA Bus level

Close to U72

Place closely to Pin 13.

Place closely to Pin 14

Place C994, C952~C957 close to Codec

Notes:

Keep PVDD supply and speaker traces routed on the DGND plane.

Keep away from AGND and other analog signals

place at AGND and DGND plane

place at Codec bottom side

R162, R163, R164, R165, R166 CO-lay with U73

R1647, C1165, R1648 for jack detect of ALC290, place close to JIO1

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A External MIC

PORT B HeadPhone Out

PORT C Dock Audio

PORT D Internal SPK

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Azalia (HD) Codec

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Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

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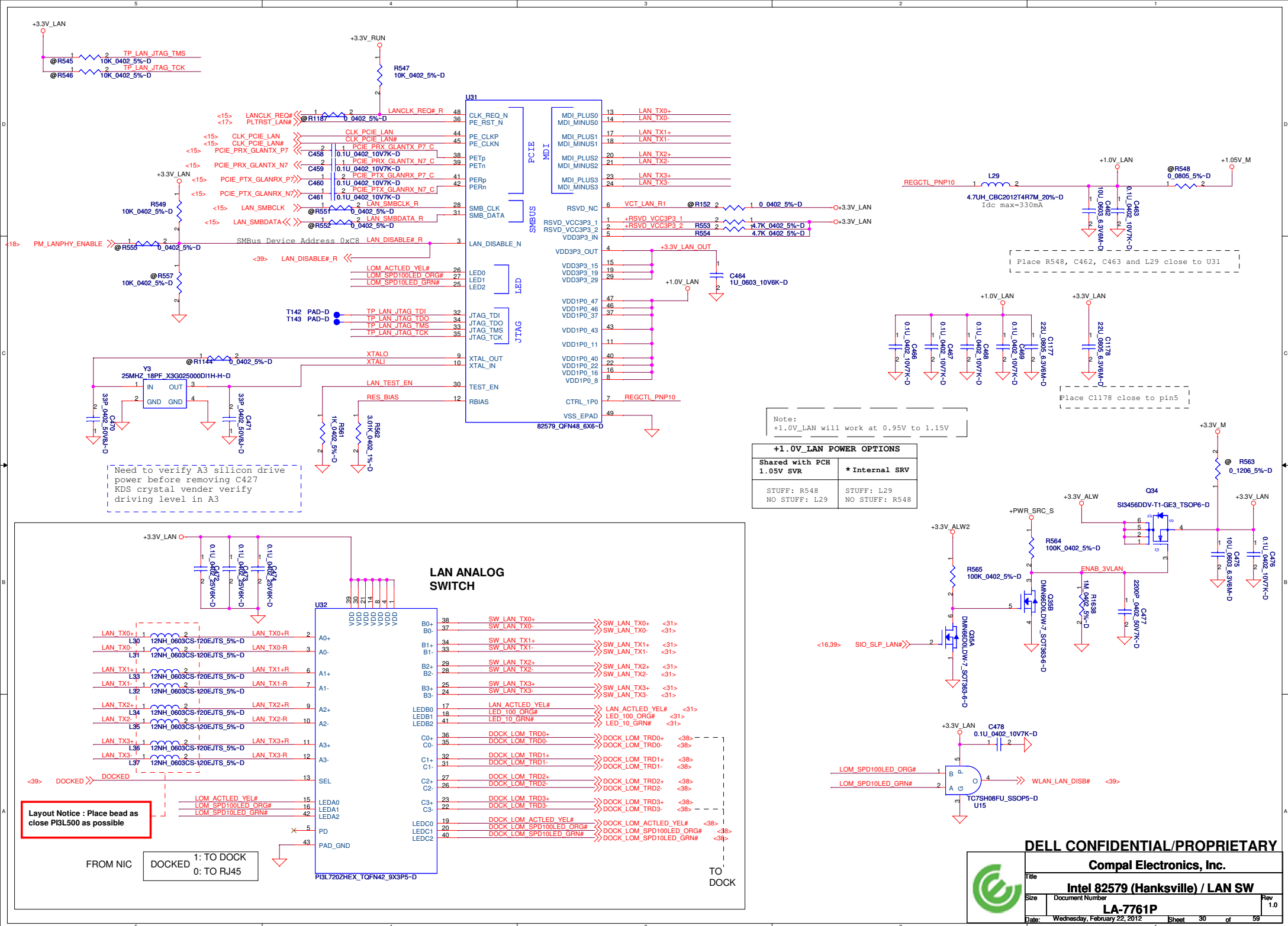
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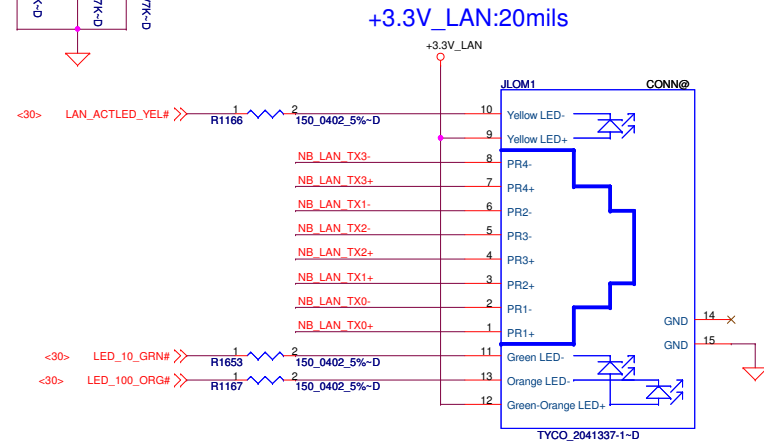
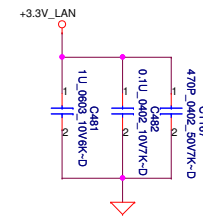
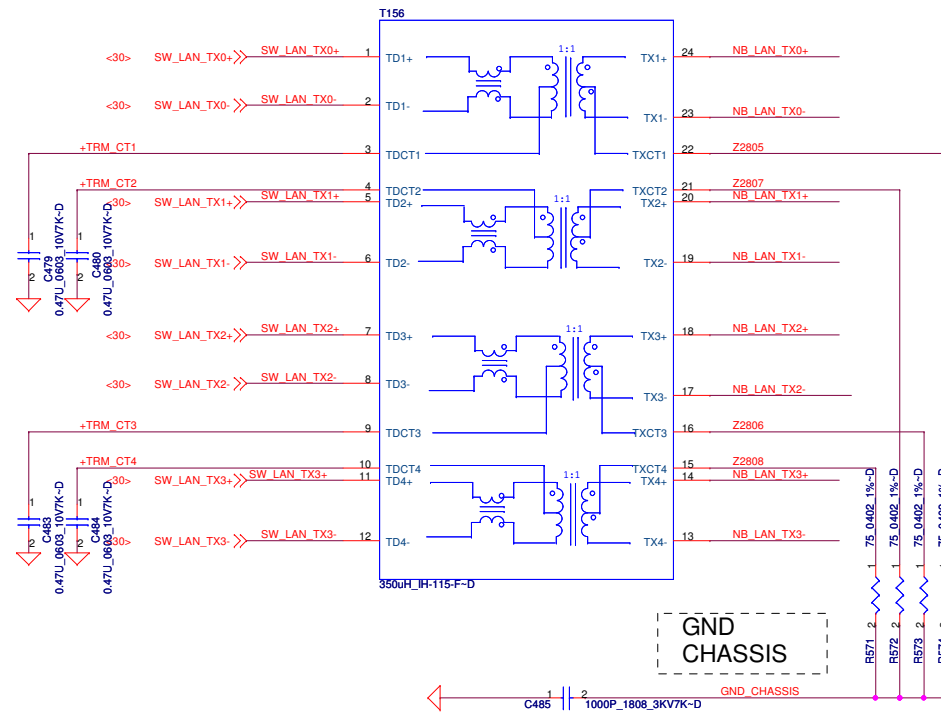
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Azalia (HD) Codec

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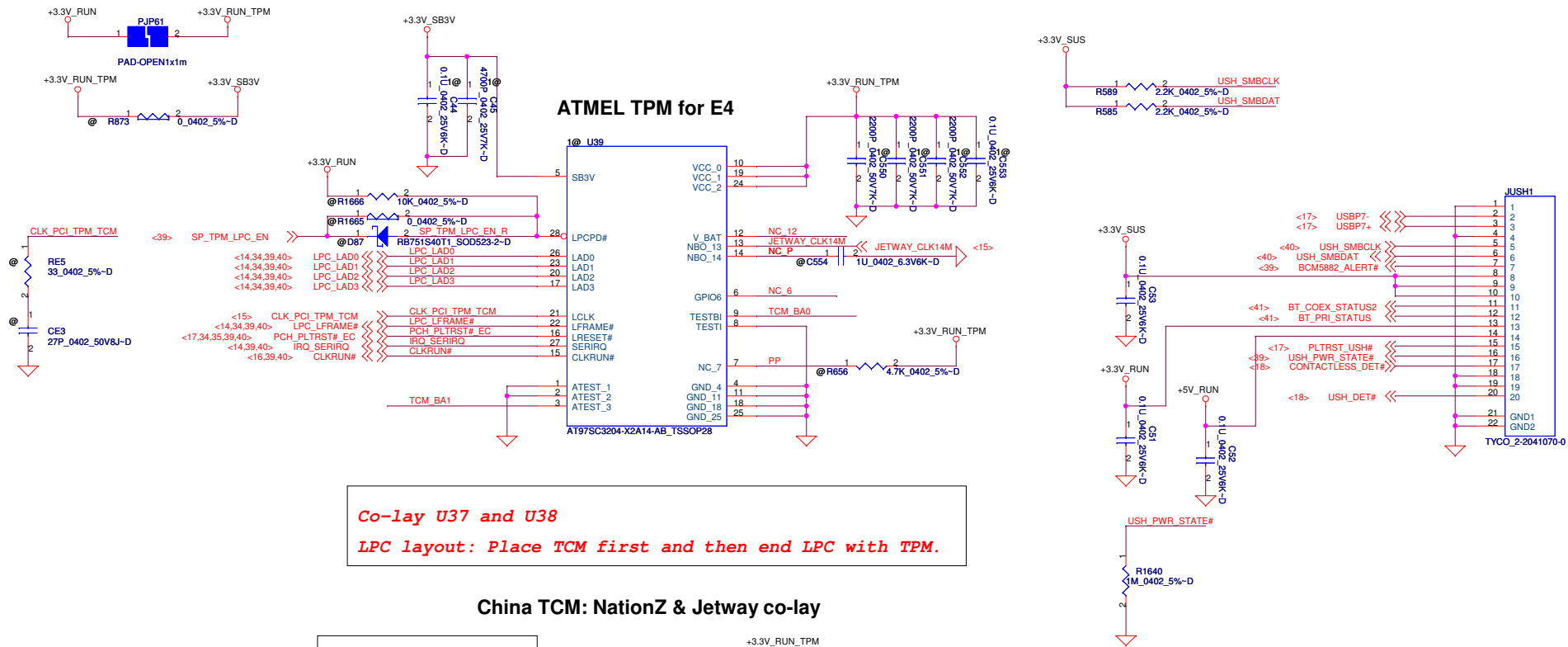


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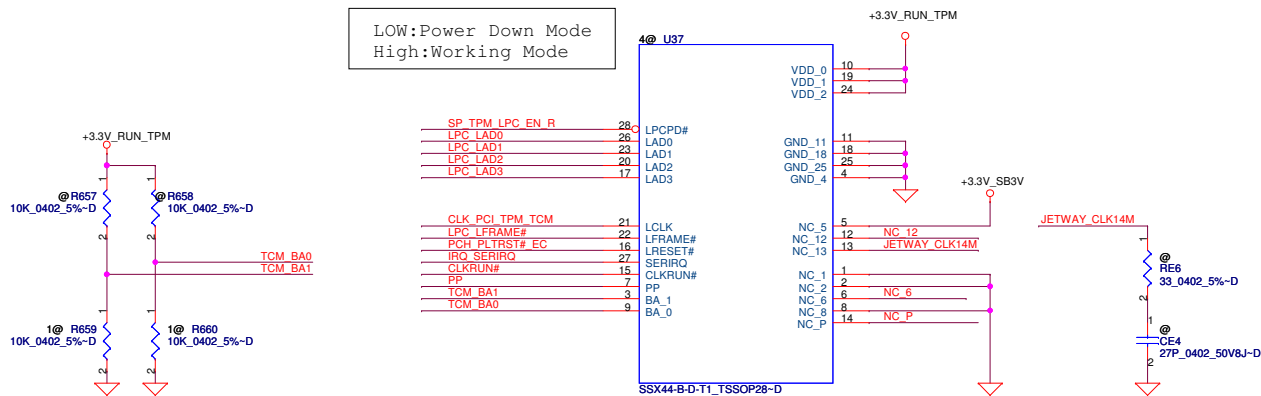
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China TCM: NationZ & Jetway co-lay

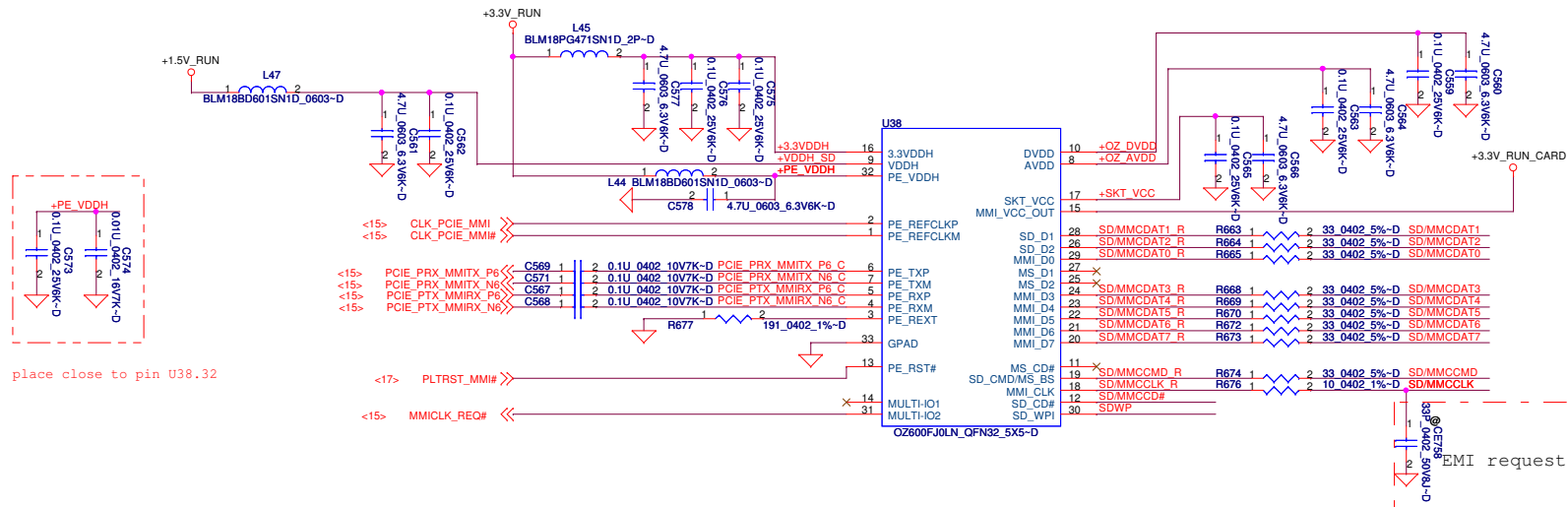


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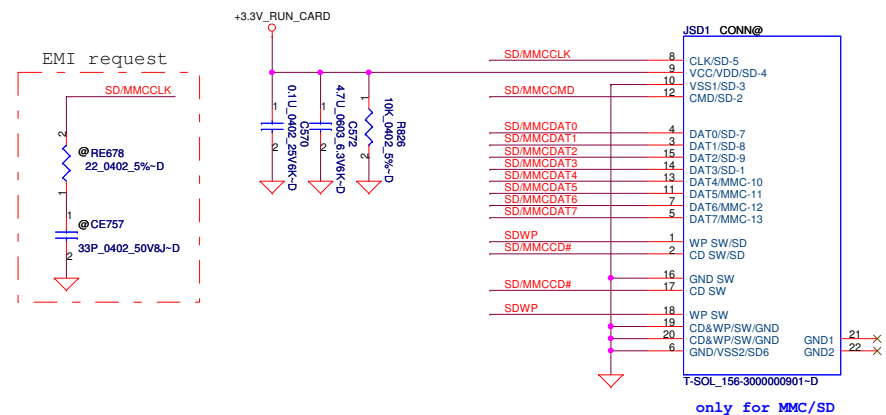
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Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



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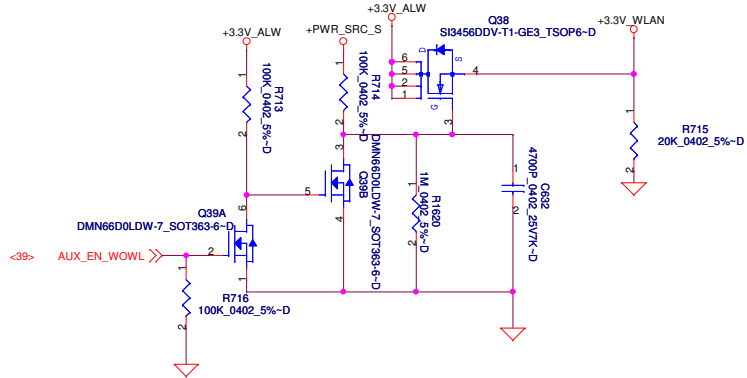
Compal Electronics, Inc.

Card Reader OZ600FJ0

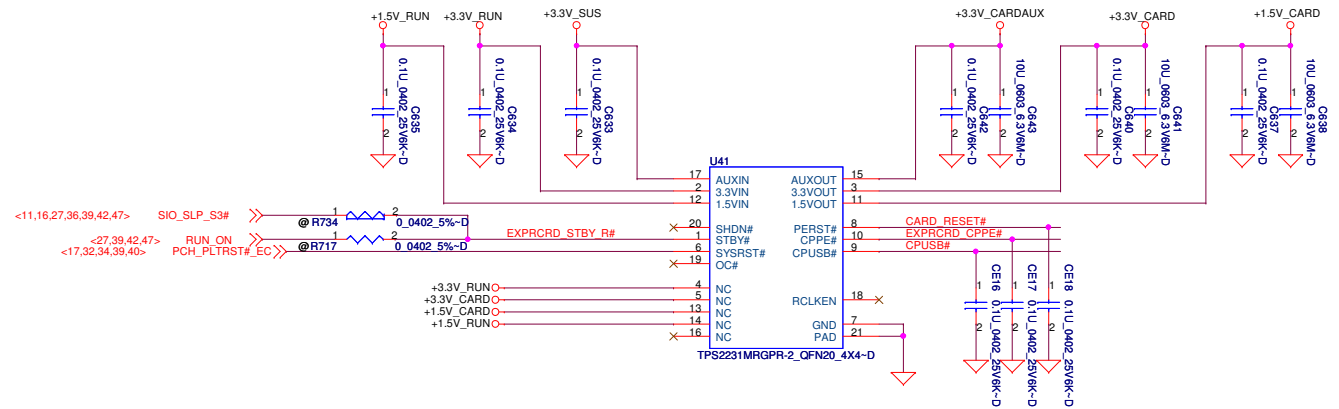
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Power Control for Mini card1

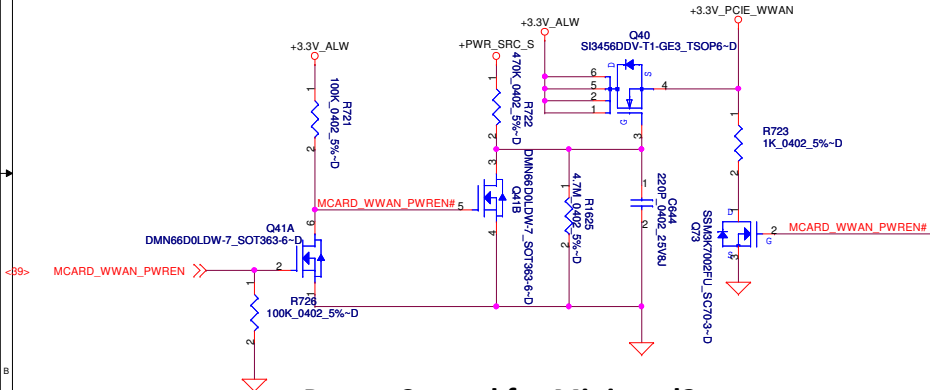


Express Card PWR S/W

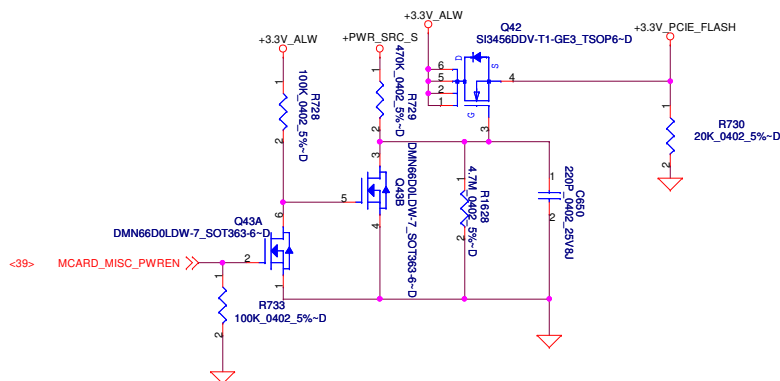


Note: Add connection on pin4, pin5, pin13 and pin14 to support GMT 2nd source part

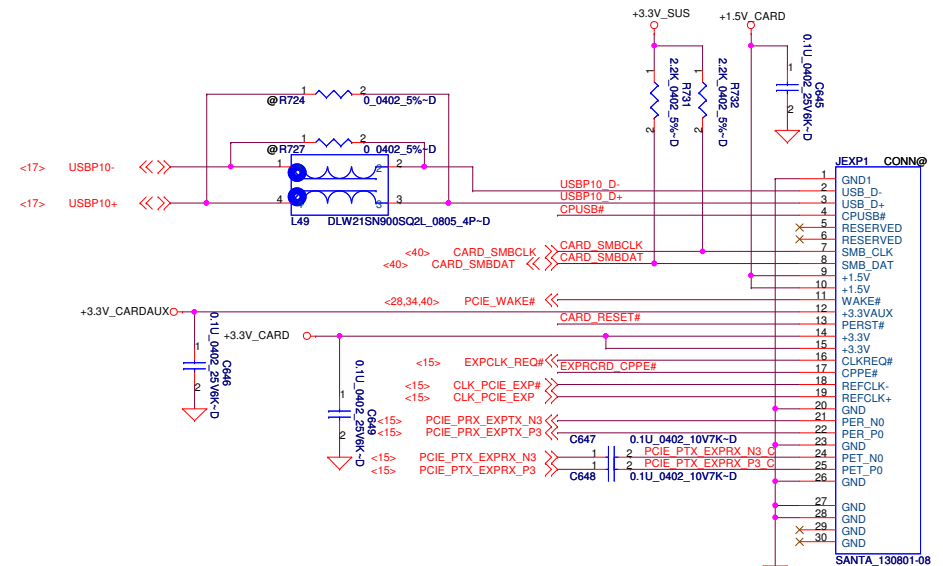
Power Control for Mini card2



Power Control for Mini card3



Express Card Conn.



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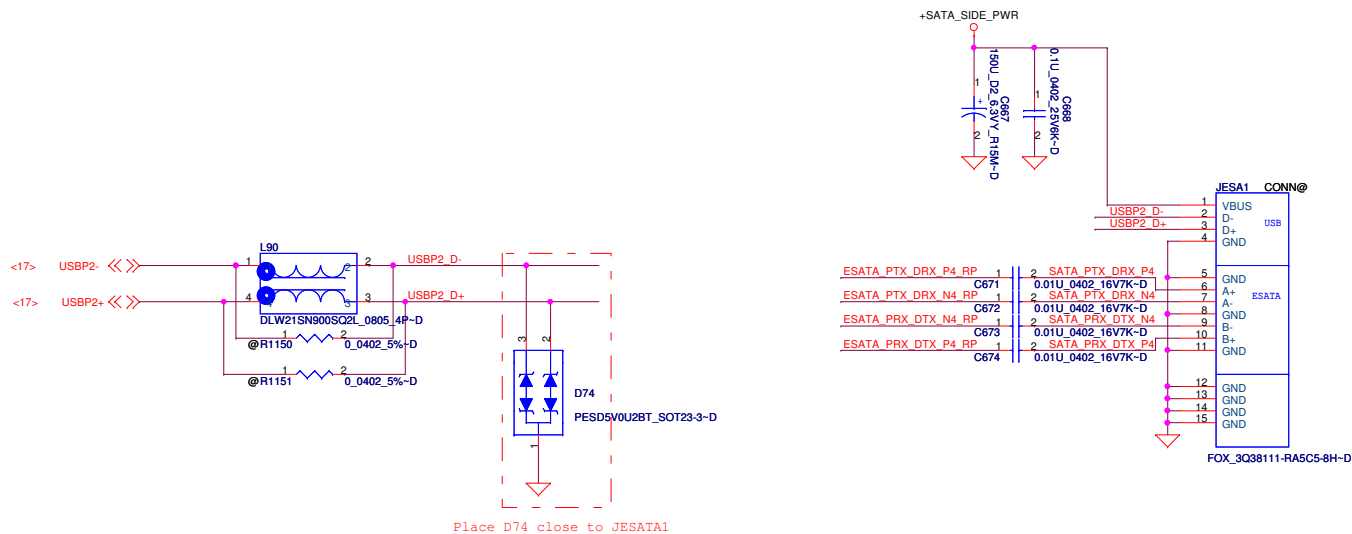
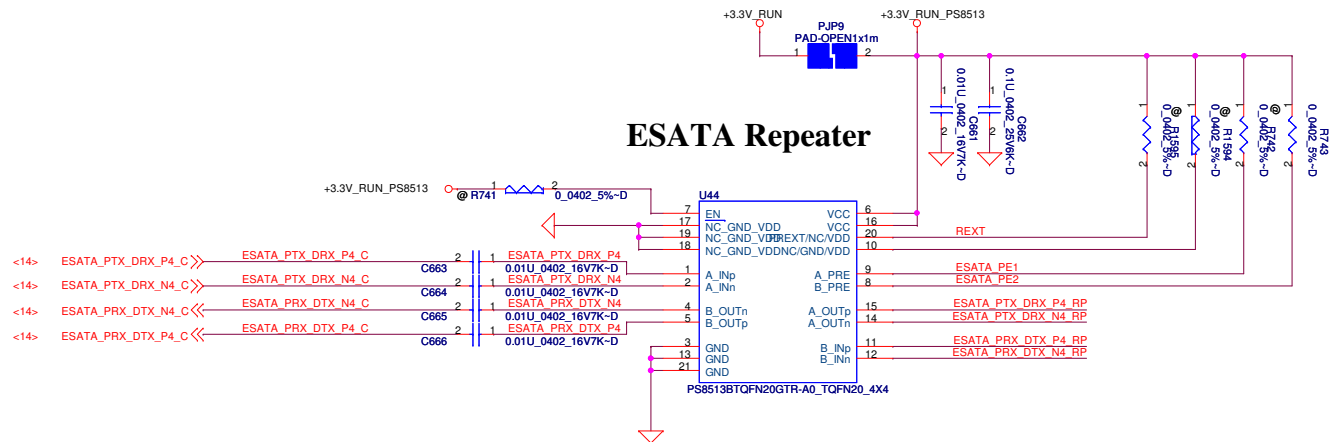
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PCIE-SATA SW / PCIE PWR

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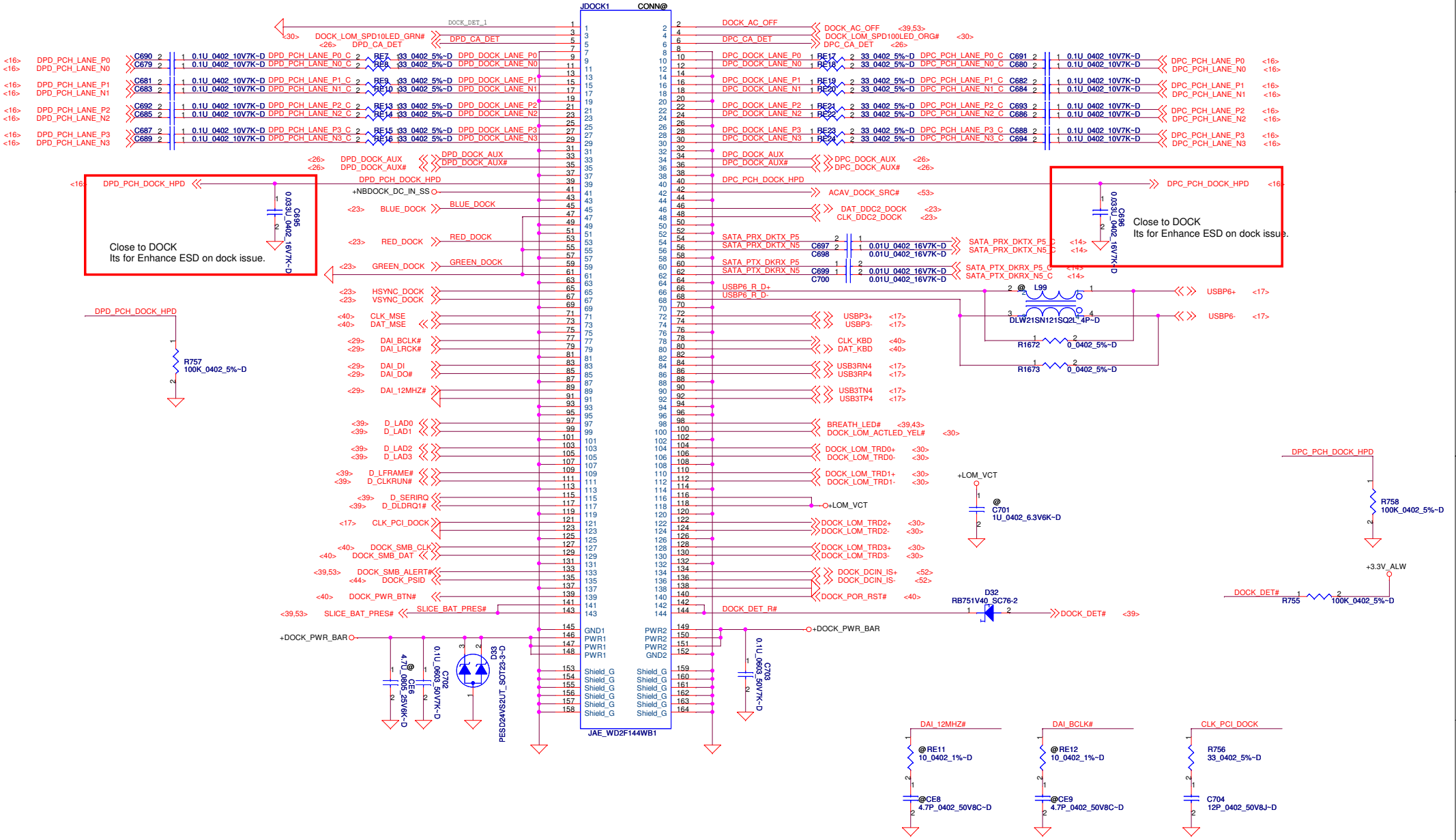


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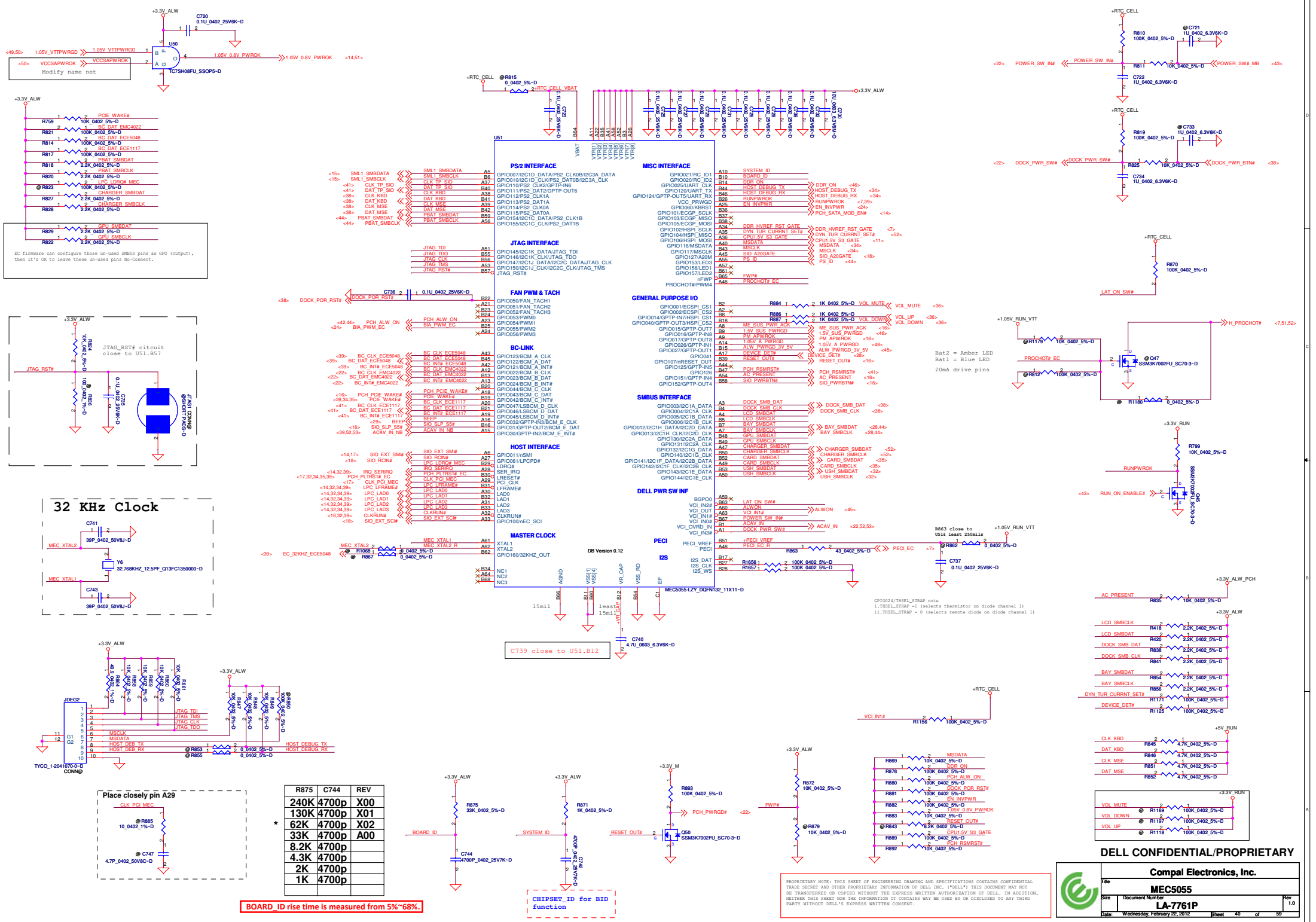
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Title				
USB/ESATA/IO/MDC				
Size	Document Number			Rev
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BOARD_ID rise time is measured from 5%~68%.

CHIPSET_ID for BID function



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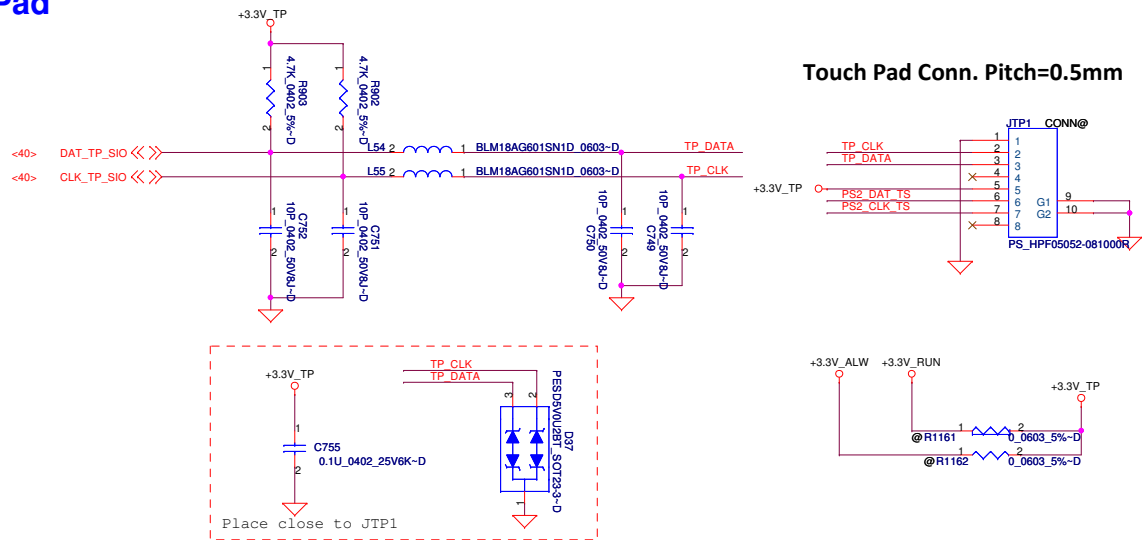
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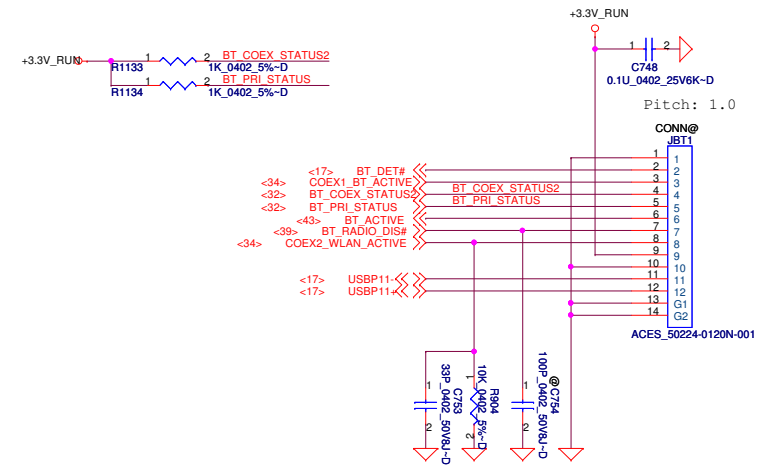
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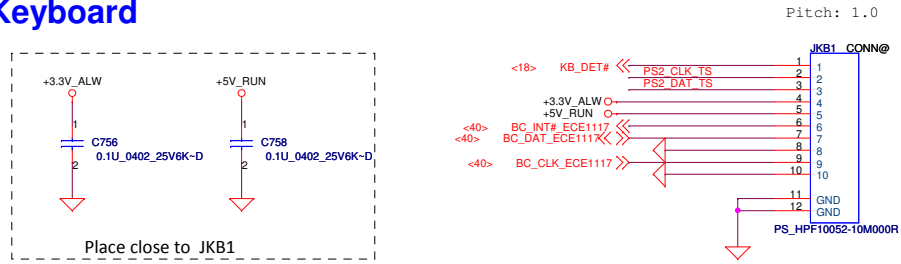
Touch Pad



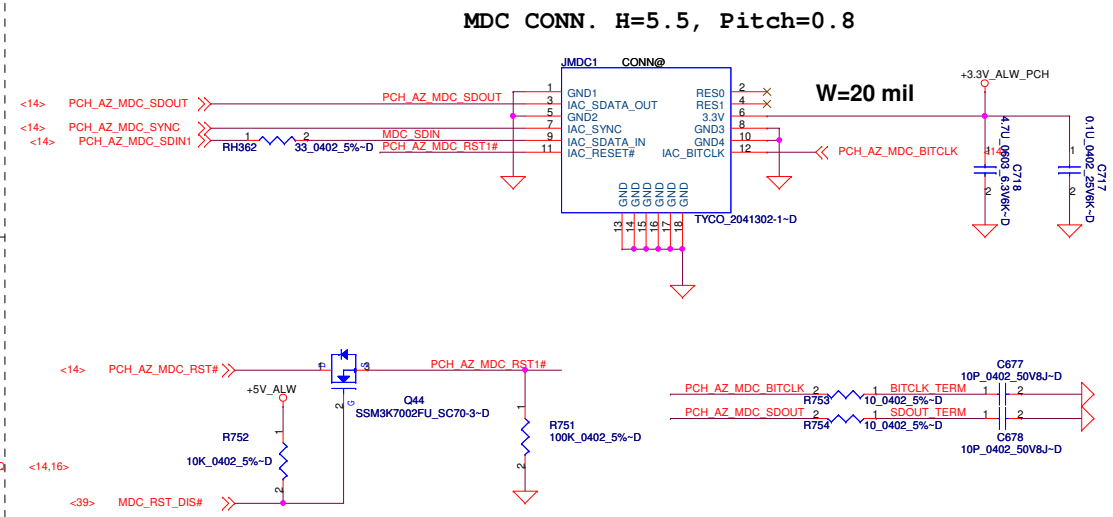
BlueTooth



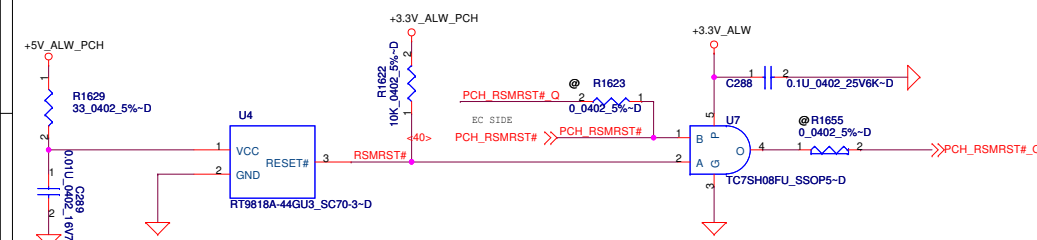
Keyboard



MDC



RSMRST#



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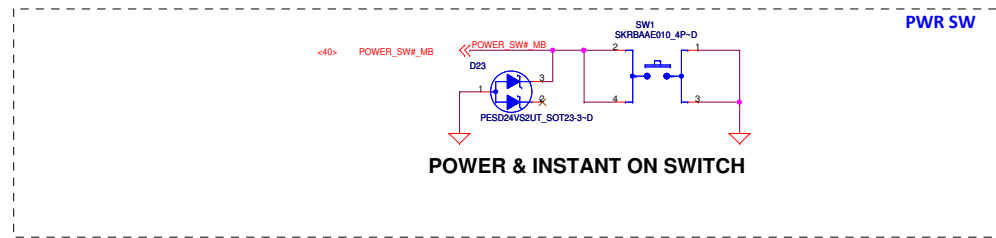
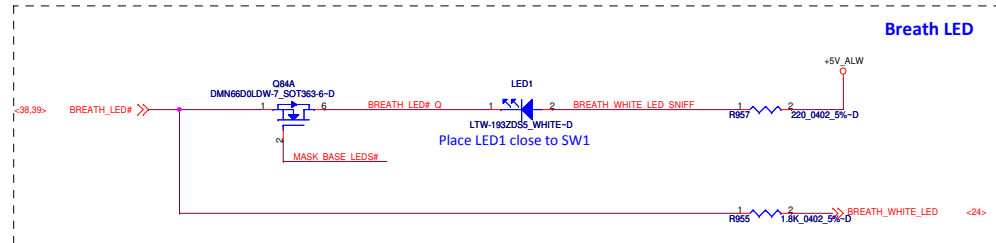
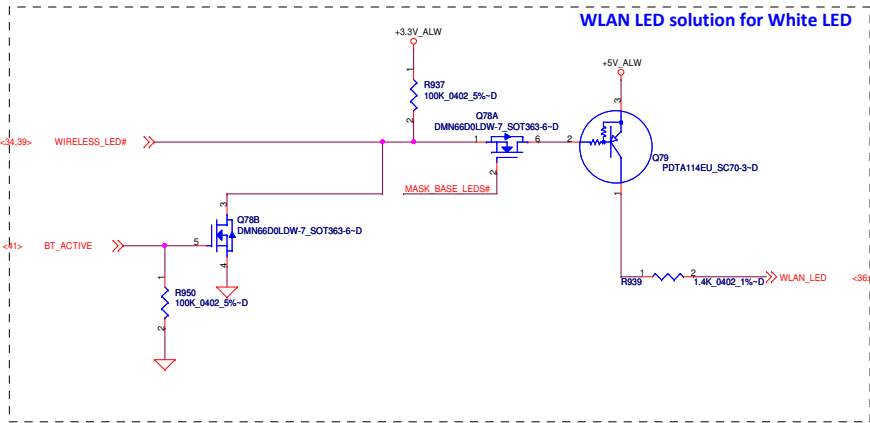
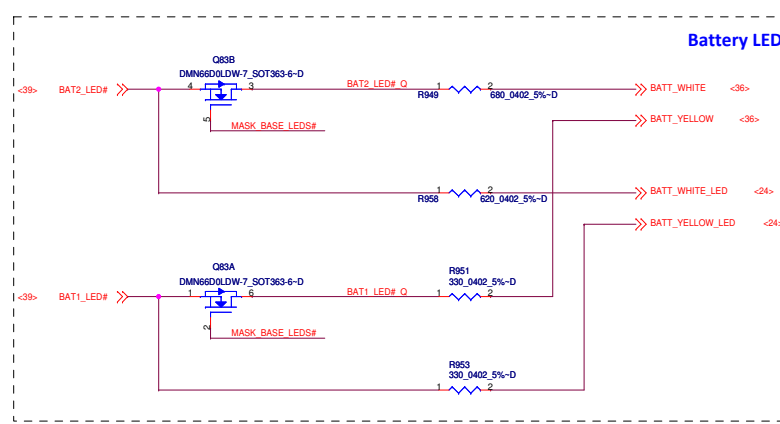
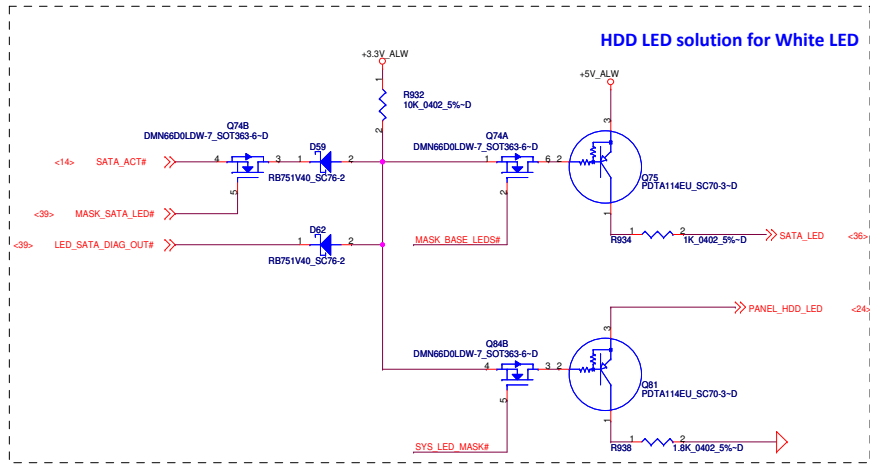


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Title		Int KB/TP/BT/RSMRST/MDC	
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The schematic diagram illustrates the power management section of the SSM3K702EPU_SCT0-3-D board. It features seven regulators (R922, R928, R923, R924, R929, R925, R926, R927) and their associated components. The regulators are connected to various input and output rails: +3.3V_SUS, +3.3V_ALW_PCH, +5V_RUN, +1.5V_RUN, +3.3V_RUN, +1.05V_RUN, +1.5V_CPU_VDDQ, and +0.75V_DDR_VTT. The diagram includes labels for the regulators, their values, and the output rails they supply. A red line indicates the RUN_ON_CPU1.5VS3# signal path.

[illegible]

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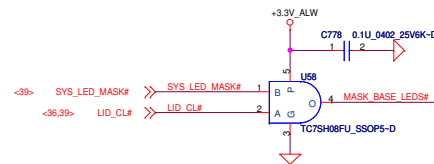
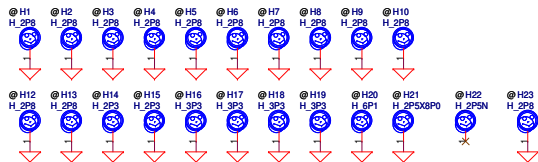


LED Circuit Control Table

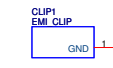
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



EMI CLIP

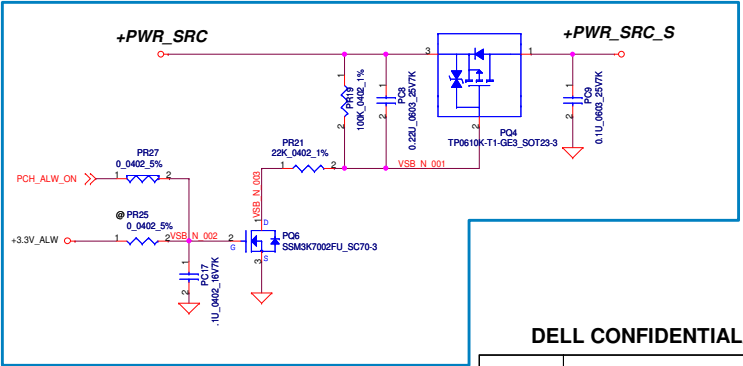
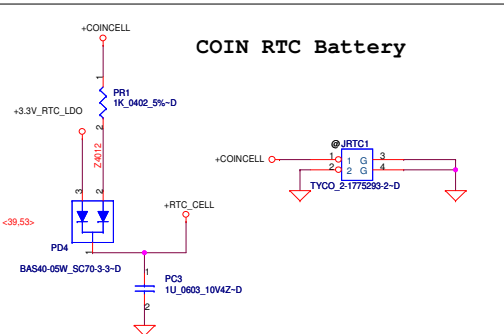
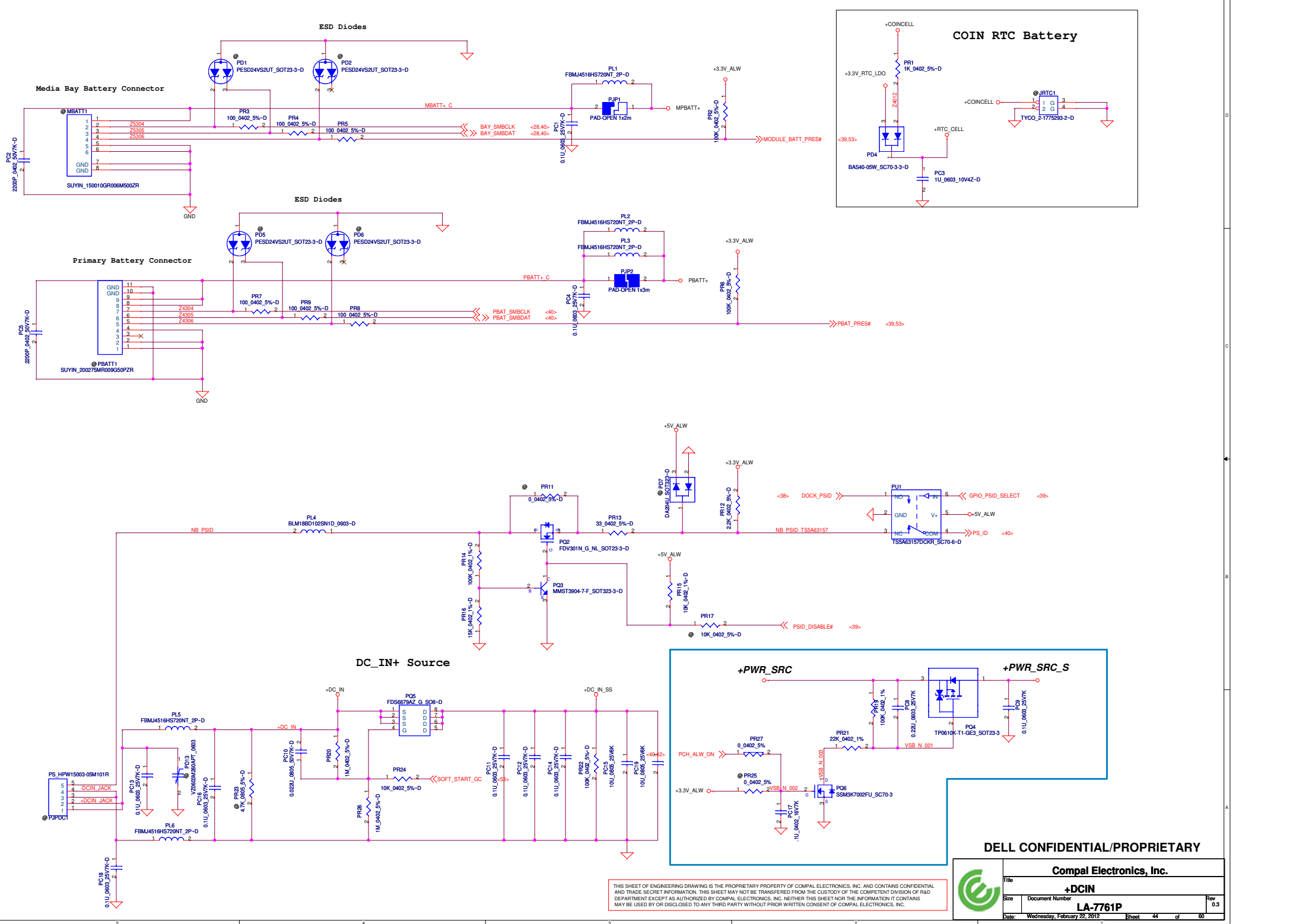


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PWR SW/LED/PAD/ME

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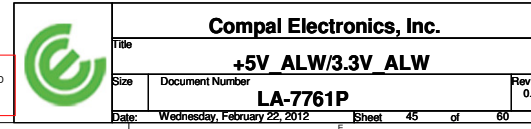
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A

Date: Wednesday, February 2

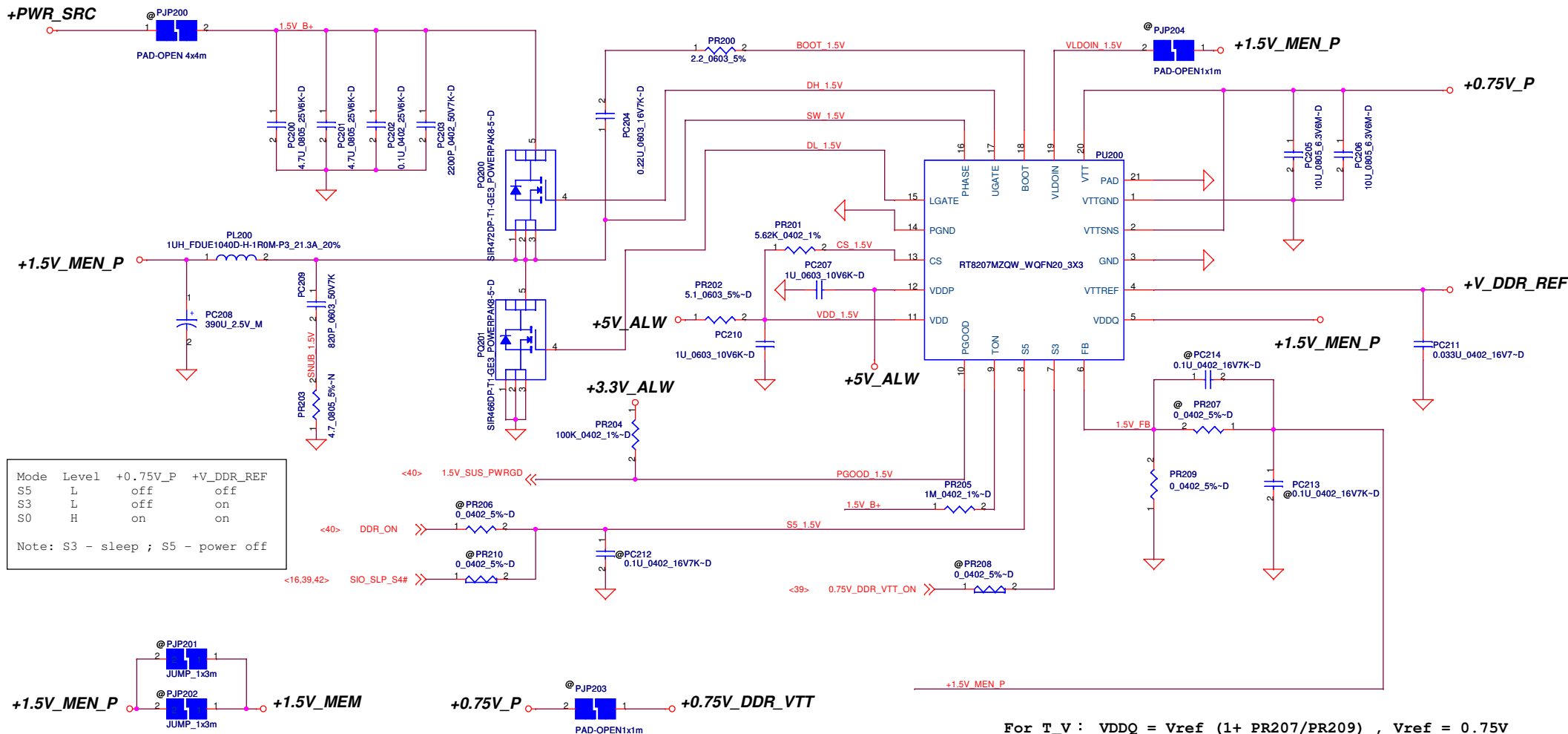


1.5V +/- 5%
TDC 7.14A
Peak Current 10.2A
OCP current 12.24A
OCP Setting 13.33A

OVP Setting 1.725V
Low side Rds(on),max 5.1m
Low side Rds(on),typ 4.2m
Choke DCR 5m
Bulk Cap ESR 10m

Frequency 300Khz

0.75V +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A
OVP Setting 0.8625V



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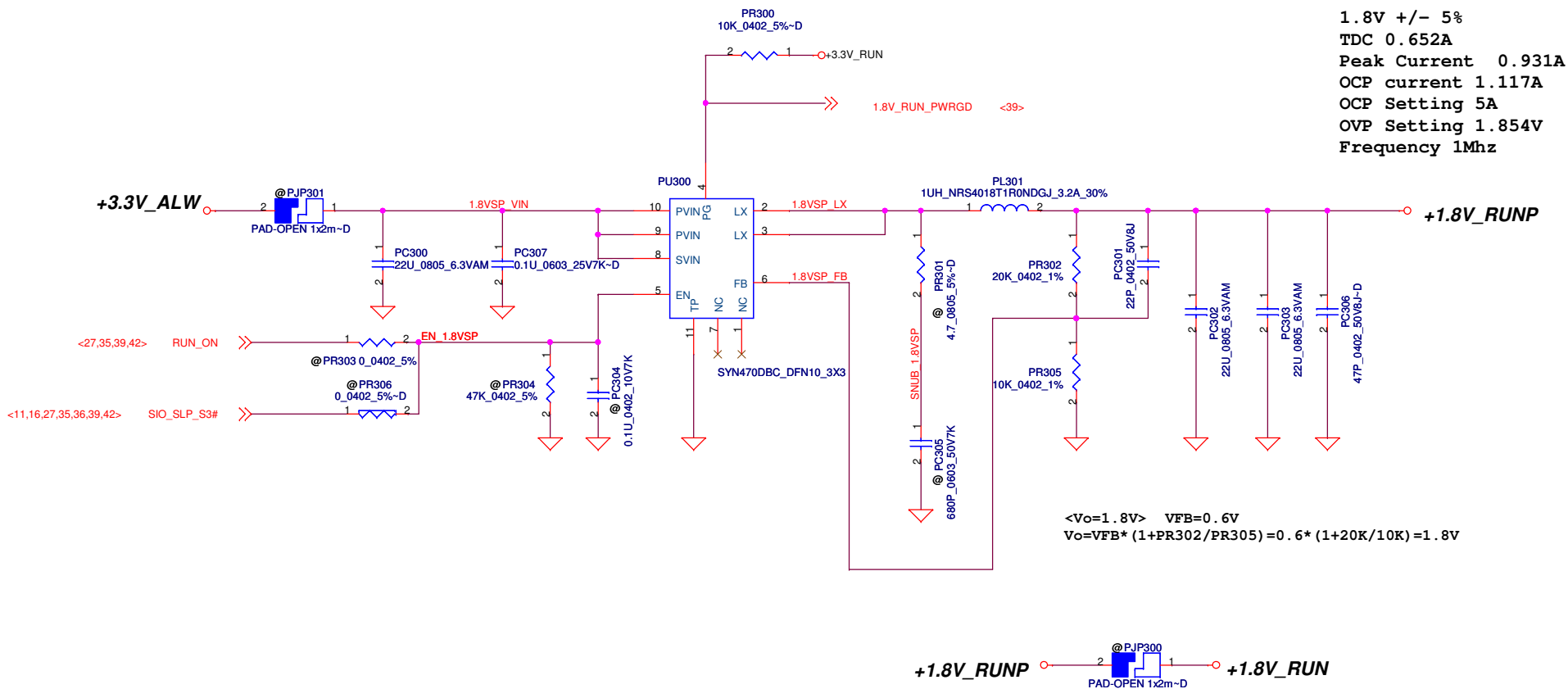
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+1.5V MEN/+0.75V DDR VTT

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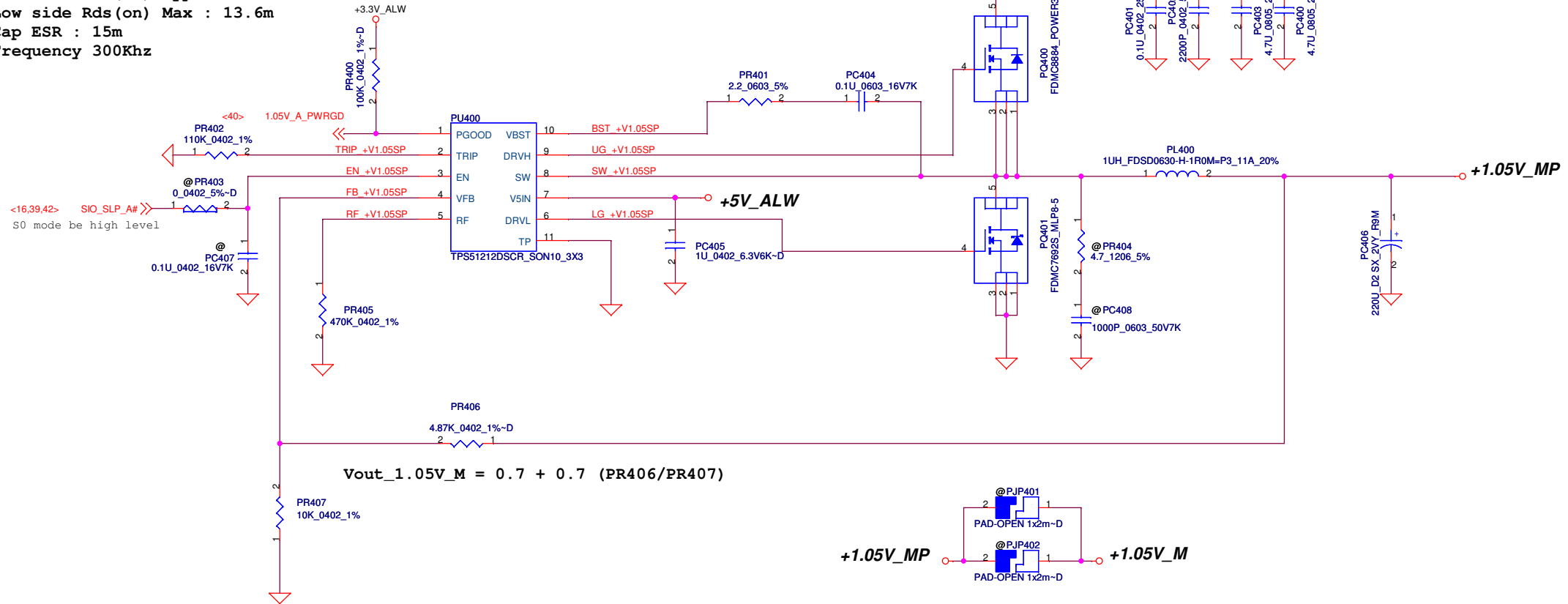


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Title			
+1.8V_RUN			
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+1.05V +/- 5%
 TDC 4.751A
 Peak Current 6.69A
 OCP setting 11.77A
 OVP Setting 1.3125V
 Low side Rds(on) Typ : 10.8m
 Low side Rds(on) Max : 13.6m
 Cap ESR : 15m
 Frequency 300Khz

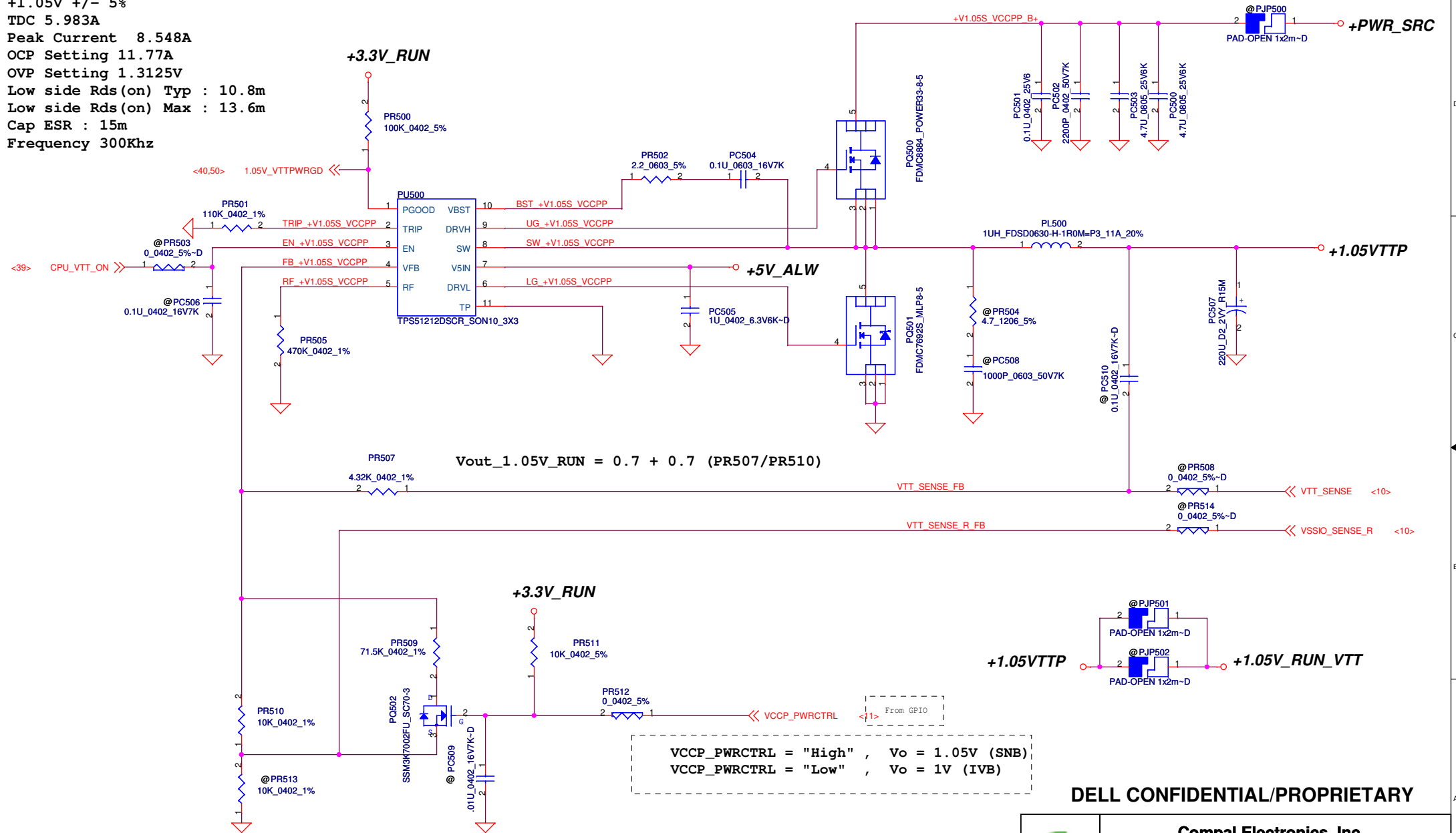


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Compal Electronics, Inc.			
Title			
+1.05V_M			
Size	Document Number		Rev
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+1.05V +/- 5%
 TDC 5.983A
 Peak Current 8.548A
 OCP Setting 11.77A
 OVP Setting 1.3125V
 Low side Rds(on) Typ : 10.8m
 Low side Rds(on) Max : 13.6m
 Cap ESR : 15m
 Frequency 300Khz



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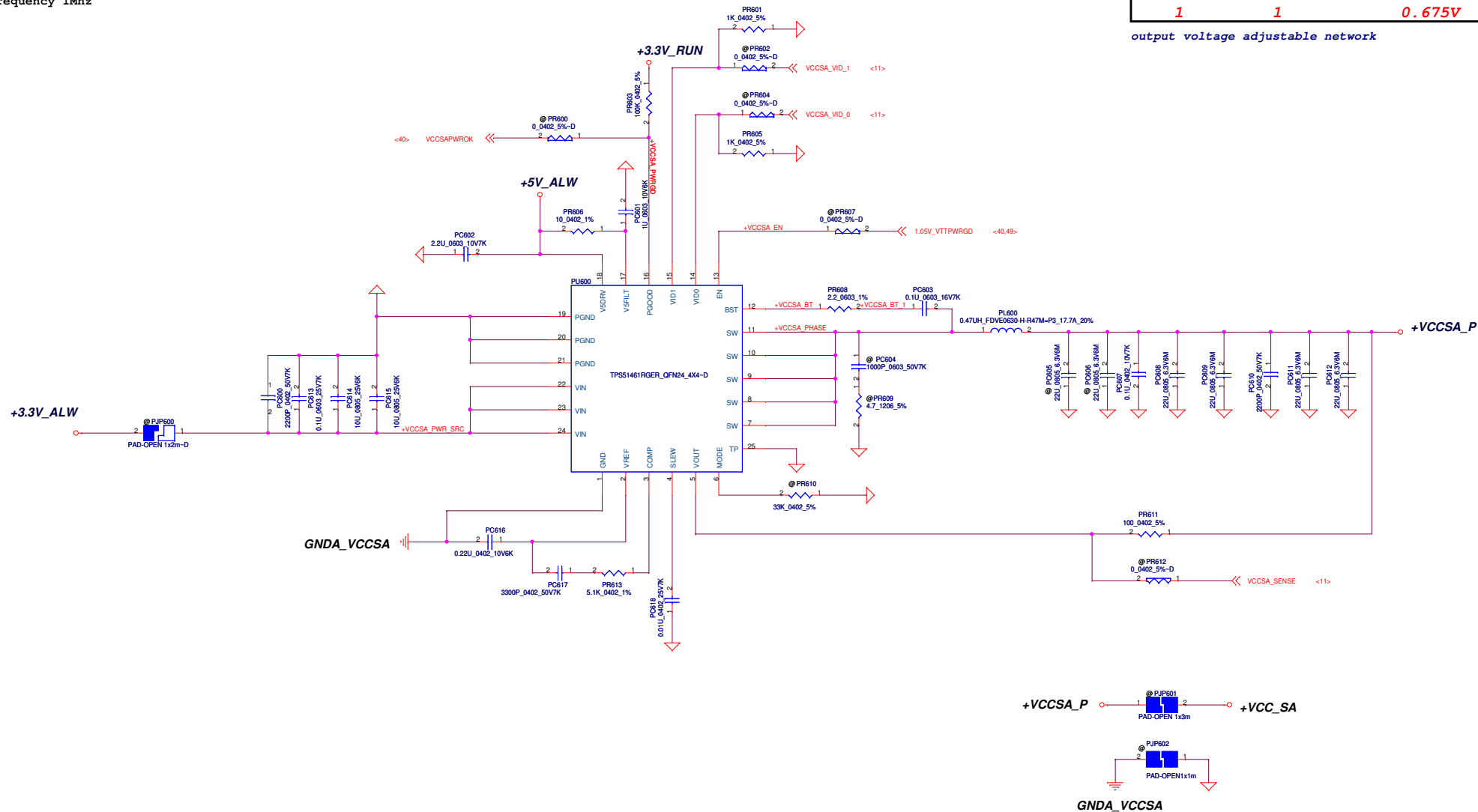
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Title		
+1.05V_RUN_VTT		
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VCCSA + / - 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OCP Settting 6.75A
OVP Setting VCCSA*120%
Frequency 1Mhz

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



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+VCC_SA

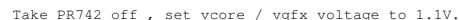
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Rev	0.5
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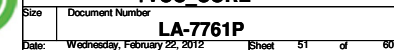
Date: Wednesday, February 22, 2012 Sheet 50 of 60

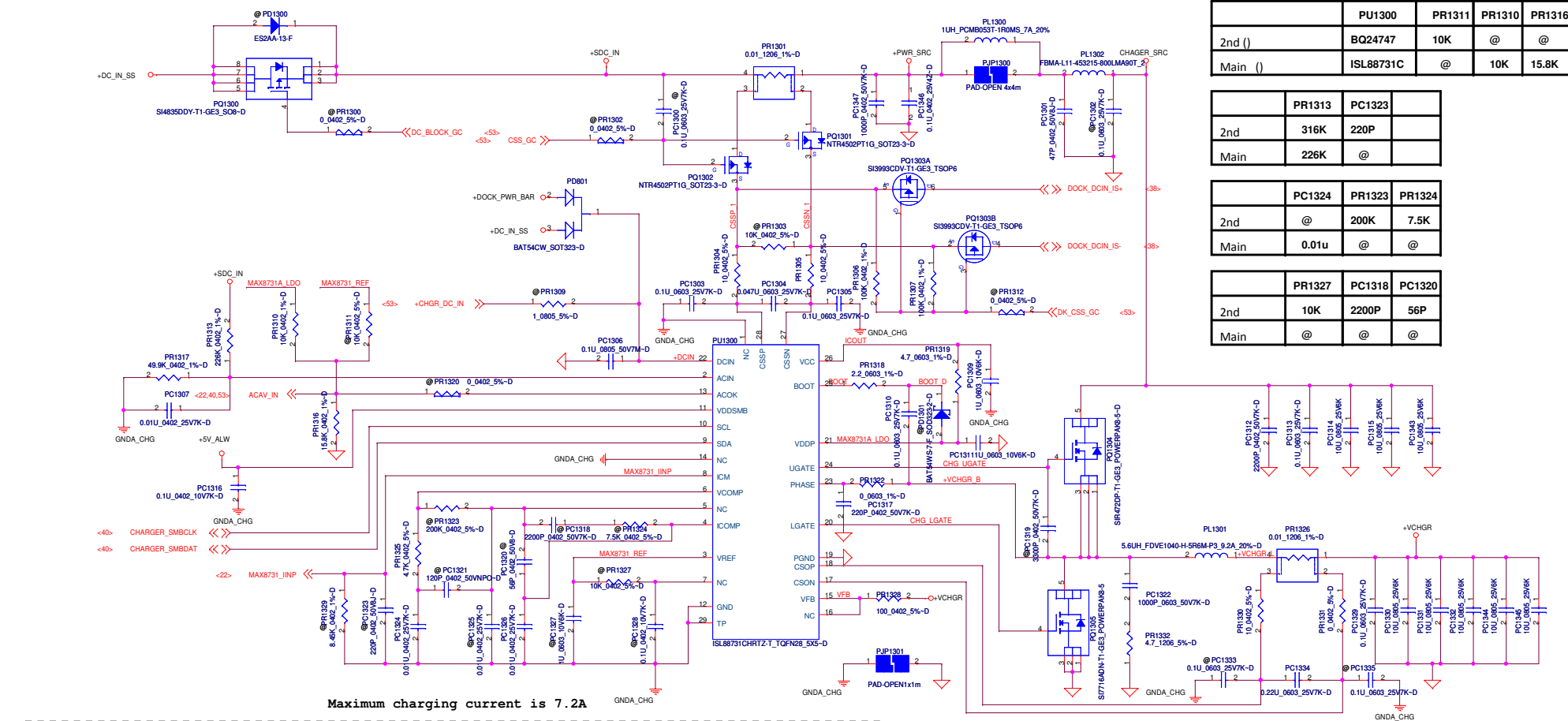
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Vcore Output Cap : 470u ESR 4.5m 4pcs
10u 0805 10pcs / 22u 0805 16pcs



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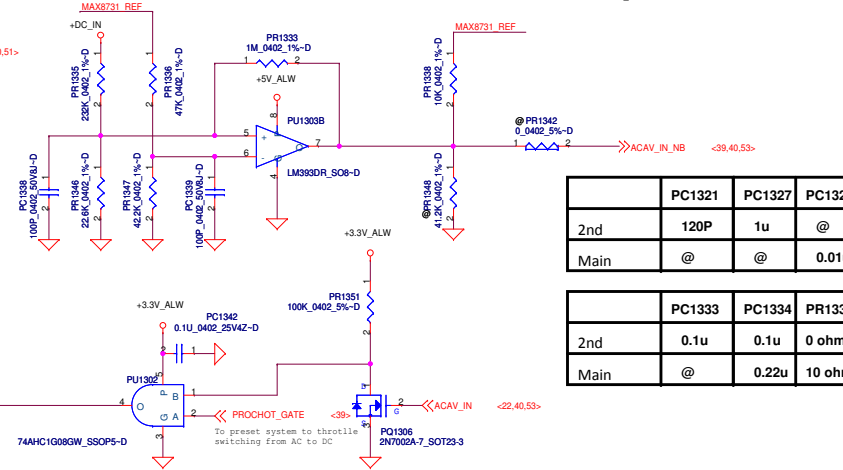
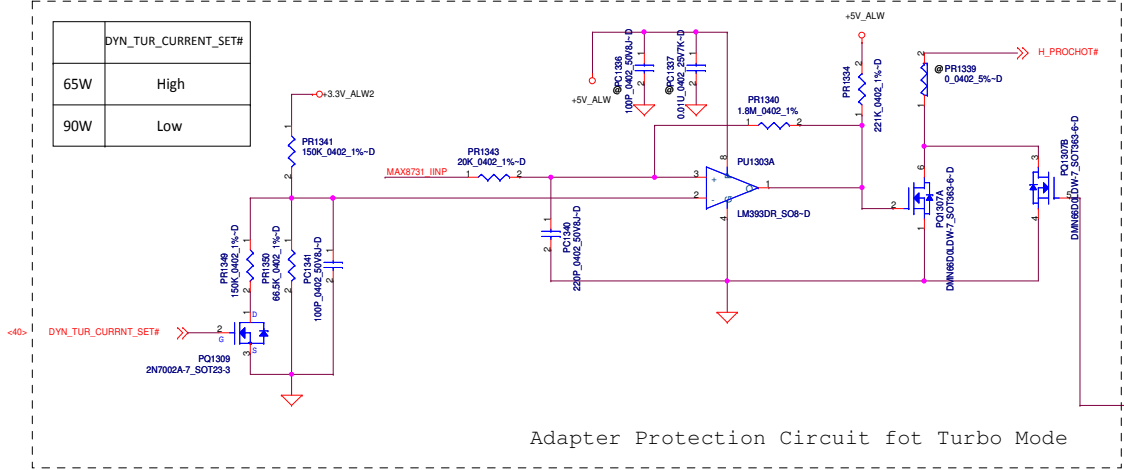


	PU1300	PR1311	PR1310	PR1316
2nd ()	BQ24747	10K	@	@
Main ()	ISL88731C	@	10K	15.8K

	PR1313	PC1323	
2nd	316K	220P	
Main	226K	@	

	PC1324	PR1323	PR1324
2nd	@	200K	7.5K
Main	0.01u	@	@

	PR1327	PC1318	PC1320
2nd	10K	2200P	56P
Main	@	@	@



	PC1321	PC1327	PC1326
2nd	120P	1u	@
Main	@	@	0.01u

	PC1333	PC1334	PR1330
2nd	0.1u	0.1u	0 ohm
Main	@	0.22u	10 ohm

	PR1322	PR1319	PC1309	PC1305	PR1304	PR1305	PC1304
2nd	1 ohm	@	@	@	0 ohm	0 ohm	0.1u
Main	0 ohm	4.7 ohm	1u	0.1u	10 ohm	10 ohm	0.047u

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Charger
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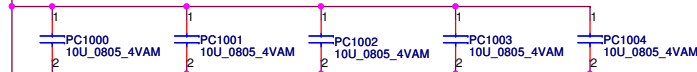
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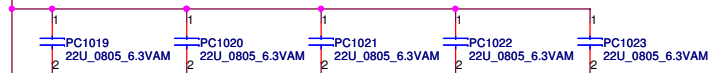
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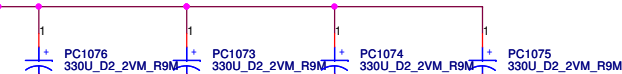
+VCC_CORE



+VCC_CORE



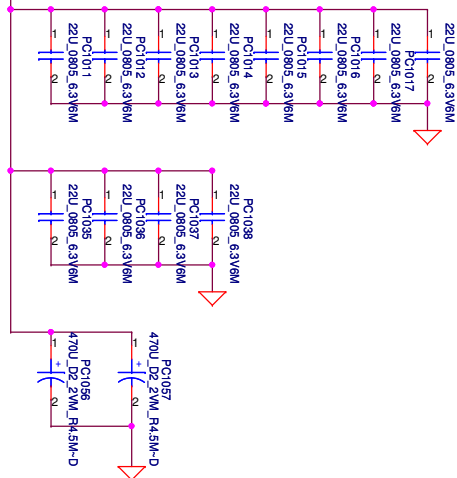
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE

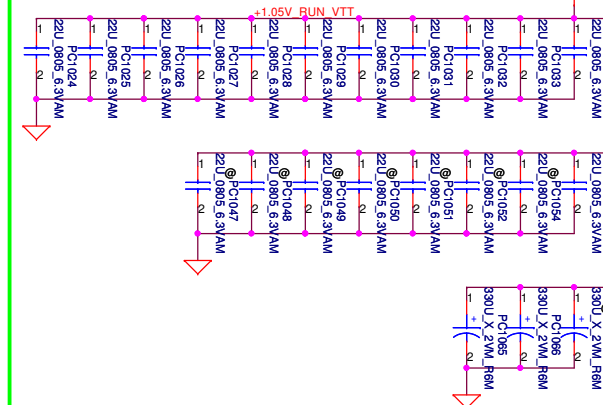
+VCC_GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05V_RUN_VTT



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Title

PROCESSOR DECOUPLING

Size Document Number

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	36	HW	6/21/2011	COMPAL	USB3.0 & E-SATA behavio error.	U48 pin 10 & pin6 swap, and pin4 & pin5 swap.	X01
2	14	HW	6/21/2011	COMPAL	SPI debug connector interfere power CAP(PC208) change connector type.	Change JSPI1 connector to SP01001DQ00.	X01
3	41	HW	6/21/2011	COMPAL	Modify Touch Pad circuit	De-pop R1162.	X01
4	11	HW	6/21/2011	INTEL	Follow INTEL check list Rev1.5.	RC99 ,RC100 change to 100 Ω.	X01
5	31	HW	6/21/2011	INTEL	Follow INTEL ORB board.	Add CC178,CC179,CC149,CC150 0.1uf 0402 caps from +1.5V_CPU_VDDQ to 1.5V_MEM power rail.	X01
6	29	HW	6/21/2011	IDT	IDT request.	PJP62 change to "JUMP_43X118".	X01
7	34	HW	6/21/2011	COMPAL	Modify WWAN circuit.	JMINI1 pin1 contact to PCIE_WAKE#.	X01
8	42	HW	6/27/2011	COMPAL	Follow E4 VC +3.3V_SUS Source circuit .	Reserve SIO_SLP_S4# contact to Q53 pin2.	X01
9	29	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify Codec circuit.	Remove R167 & R178 (0 Ω) .	X01
10	18	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify PCH_GPIO16 pull-up resistor.	Change RH272 from 100KΩ to 10KΩ.	X01
11	17	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify CAM_MIC_CBL_DET# pull-up resistor.	Change RH331 from 8.2KΩ to 10KΩ.	X01
12	42	HW	7/28/2011	COMPAL	Load SW sources output rising time mismatch and COS.cost concern.	Change back to E3 +3.3V/5V_RUN discrete solution	X01
13	15	HW	7/28/2011	COMPAL	bass on vender measure crystal EA by pass.	CH18,CH19 change to 10pF.	X01
14	34	HW	7/28/2011	COMPAL	Follow INTEL check list (Rev1.5) change PCH GPIO52(PCIE_MCARD2_DET#) pull up resistor to 10KΩ.	Change R695 from 100K to 10Kohms.	X01
15	32	HW	7/28/2011	COMPAL	INTEL power sequence fail on T13(+1.8V_RUN to H_CPUPWRGD assert) due to USH move to sub-board but "USH_PWR_STATE#" no PU/PD for default.	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
16	11	HW	7/28/2011	COMPAL	Follow INTEL check list Rev1.5 for "VCCIO_SEL" , series resistor no stuff .	De-pop RC140	X01
17	11	HW	7/28/2011	COMPAL	CH94 and CH95 to D2 size for cost concern	Change CH94 and CH95 from SGA0000170L to SGA00004L0L	X01
18	22	HW	7/28/2011	COMPAL	Thermal solution change to EMC4021 for cost concern.	Change thermal sensor to EMC4021 for UMA	X01
19	29	HW	7/28/2011	COMPAL	Codec is change to 92HD93.	Pop R162~R166 and de-pop U73	X01
20	40	HW	7/28/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
21	20,43	HW	7/28/2011	COMPAL	Turn on +5V_ALW_PCH MOSFET Vgs less than cut-in voltage in battery mode.	Add control circuit for +5V_ALW_PCH	X01
22	14,40	HW	7/28/2011	COMPAL	SMSC no support function for LPC_LDRQ0#.	Delete net, LPC_LDRQ0#. Leave LDRQ0# no connection on both of 5048 and PCH side	X01

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Title EE P.I.R (1/3)		
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	29	HW	7/28/2011	IDT	CODEC is change to 92HD93.	Pop R162~R166 and de-pop U73	X01
24	29	HW	7/28/2011	IDT	Co-lay 92HD93 circuit for I2S BUS control.	Reserve 0 Ω to connect Codec(92HD93) Pin48 for EN_I2S_NB_CODEC#.	X01
25	42	HW	8/3/2011	COMPAL	Modify +1.5V_RUN load switch circuit for POWER team suggestion.	Change Q59 from NTGS4141NT1G to AO4728L.	X01
26	43	HW	8/3/2011	COMPAL	Follow INTEL Power down sequence Tc timing fail(BITS:DF493966).	Add AND Gate(TC7SH08FU) input connect PM_APWROK & SIO_SLP_A# , and output connector PM_APWROK_R.	X01
27	23	HW	8/4/2011	TI	CRT SW for TI 2nd source.	U18.29 connect to +3.3V_RUN.	X01
28	41	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
29	17	HW	8/4/2011	COMPAL	Intel Review Feedback for PCH_GPIO3.	POP RH332.	X01
30	30	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Modify codec schematics	X01
31	25	HW	8/8/2011	COMPAL	Add HDMI repeater.	Modify HDMI circuit.	X01
32	17	HW	8/11/2011	COMPAL	RF request.	1.CLK_PCI_MEC add By pass 10p after 22ohm(RH102) 2.CLK_PCI_LOOPBACK add By pass 10p after 22ohm(RH105)	X01
33	43	HW	8/11/2011	COMPAL	White light LED brightness is abnormal	change the resistor value: R934 change to 1K,R938 & R955 change to 1.8K,R939 change to 1.4K,R949 & R958 change to 620 and R957 change to 220.	X01
34	11	HW	8/12/2011	COMPAL	S3 resume issue.	Pop RC79 and de-pop RC82	X01
35	36	HW	8/29/2011	COMPAL	USB3.0 Tx AC coupling follow CRBboard.	change C412 & C413 to 0.1uF.	X01
36	19	HW	8/29/2011	COMPAL	CRT ripple garbage display issue.	change LH1 to 1uH inductor.	X01
37	43	HW	8/29/2011	COMPAL	White light LED brightness is abnormal	change the resistor value from 2.2K to 1.2K for R949, R958, R957, R955, R939, R938, R934	X01
38	29	HW	9/28/2011	COMPAL	Audio no sound issue in Dalmore 15 UMA. (BITS:DF504001).	Add C-R snubber circuit,C973~C976 (2200P),R1658~R1661 (3.3 Ω)	X02
39	40	HW	9/28/2011	COMPAL	EC has internal pull up for volume signals.	De-pop R1169, R1197, R1118.	X02
40	42	HW	9/28/2011	COMPAL	+3.3V_RUN boot leakage issue.	Pop Q69 & R929.	X02
41	39	HW	9/29/2011	COMPAL	SMSC change ECE5048 Pin A23 to GPIO0.	Link ECE5048 symbol.	X02
42	25	HW	10/12/2011	COMPAL	Remove HDMI level shifter and change to HDMI EMI low cost solution.	Modify HDMI circuit,De-pop L19~L22. Add L100~107 (9nH) and C1209~C1216 (3.3pF).	X02
43	19	HW	10/12/2011	COMPAL	CRT ripple garbage display issue	Change CH36 from 10uF(0603) to 22uF(0805).	X02
44	33	HW	10/12/2011	COMPAL	EMI request to change SD CLK series R	R676 is changed from 33ohms to 10ohms	X02

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46	43	HW	10/12/2011	COMPAL	DFX request to change CILP PAD.	Change CLP1 PAD from "79X138" to "110X138" .	X02
47	ALL	HW	10/12/2011	COMPAL	For cost saving	Change 0 ohm resistor to short pad.	X02
48	41	HW	10/12/2011	COMPAL	SMSC review feedback.	Reserve R1656 and R1657 100Kohms to GND for I2S disabled.	X02
49	29	HW	10/12/2011	COMPAL	Remove ALC290 co-lay circuit	Remove R1646, C1164, R1644, R1643, R1642, R171, C1204, C1205, R1647, C1165, R1648 and R1645.	X02
50	39	HW	10/13/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766.	X02
51	41	HW	10/13/2011	COMPAL	Change reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.	X02
52	17	HW	10/19/2011	COMPAL	UMA PCI clock noise issue. [BITS:DF511181]	Pop CH20 & CH21 to 8.2pF.	X02
53	7	HW	10/21/2011	COMPAL	ESD Request.	Reserve 100p cap on PCH_PLTRST#_R , H_THERMTRIP#_R , XDP_DBRESET#_R, VIDSCLK and VIDSOUT .	X02
54	7	HW	10/21/2011	COMPAL	ESD Request.	Reserve 8.2p cap on CLK_PCI_5048.	X02
55	22	HW	10/25/2011	COMPAL	VSET Setting change Tp from 88 degree to 93 degree.	change R406 from 953Ω to 1.33KΩ	X02
56	38	HW	10/27/2011	COMPAL	EMI request to add 33Ω for DP port.	Add 33ohm on DPD_DOCK_LANE_P0/N0,DPD_DOCK_LANE_P1/N1,DPD_DOCK_LANE_P2/N2, DPD_DOCK_LANE_P3/N3,DPC_DOCK_LANE_P0/N0, PC_DOCK_LANE_P1/N1, DPC_DOCK_LANE_P2/N2, PC_DOCK_LANE_P3/N3.	X02
57	7	HW	10/27/2011	COMPAL	ESD Request.	RC19.2 change to XDP_DBRESET#_R. RC29.2 change to XDP_TDI_R. RC35.2 change to XDP_TDO_R.	X02
58	34	HW	11/08/2011	COMPAL	PCH GPIO52 changed to be free.	De-pop R725, remove R695 and add RH359.	X02
59	ALL	HW	11/08/2011	COMPAL	For cost saving	Change 1Kohms +-1% to +-5% except RC78, RC80, RC81 and RC84.	X02
60	11, 43	HW	11/14/2011	COMPAL	AO4728L leakage issue	Change QC3 and Q59 to AO4304L (SB00000RV00).	X02
61	32	HW	11/14/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Add D87, R1666 and R1665 for HW solution backup.	X02
62	11,24,29.	HW	11/16/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 330K to 470K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p	X02
63	40	HW	11/16/2011	COMPAL	Change PCH to C1 version.	Change UH4 to SA00005BU1L.	X02
64	14~21	HW	11/16/2011	COMPAL	Change board ID to X02.	Change R875 to 62Kohms.	X02


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65	17, 34, 38.	HW	12/05/2011	COMPAL	EMI request for USBP6 & USBP8. [BITS:DF524330]	Swap USB Port6 and Port8 and reserve a choke at E-Docking conn. side: Port6 from Mini3 Pink Panther card to E-docking Port8 from E-Docking to Mini3 Pink Panther card	X02
66	35	HW	12/05/2011	COMPAL	EMI request to add 0.1u CAP for Express Card.	Add 0.1u CAP on EXPRCRD_CPPE#, CARD_RESET#, CPUSB# traces.	X02
67	24	HW	12/06/2011	COMPAL	EMI request for USBP12. [BITS:DF524330]	Pop L10 and De-pop R427, R428.	X02
68	25	HW	12/06/2011	COMPAL	EMI final solution for HDMI.	C1209~C1216 CAP 3.3P Change to 1.8PF, OB 680 change to 604ohm.	X02
69	40	HW	02/01/2012	COMPAL	Change board ID to A00.	Change R875 to 33Kohms.	A00
70	17	HW	02/01/2012	COMPAL	33MHz PCI noise.	Modify CLK_PCI_MEC and CLK_PCI_Loopback damping(RH102 and RH105) from 22ohm to 33ohm.	A00
71	42	HW	02/20/2012	COMPAL	ME Request.	SW1 change to SN11100580L.	A00
72	All	HW	02/20/2012	COMPAL	For cost saving.	Change 0 ohm resistor to short pad, total 15 pcs.	A00
73	27	HW	02/20/2012	COMPAL	For cost saving.	HDD PWR De-pop :R1624, R500, R499, R504, R516, Q28, C393, C394.	A00
74	14	HW	02/20/2012	COMPAL	For cost saving.	De-pop RH288, RH48, RH49, RH47.	A00
75	7	HW	02/20/2012	COMPAL	ESD Request.	De-pop RC30, RC31, RC33, RC34, RC36, RC37, RC38, RC39 .	A00
76	36	HW	02/20/2012	COMPAL	System will reconnect USB 3.0 after resume from S3 issue. [BITS:DF537410].	JBTB1 Pin 38 reserve R154 to +3.3V_ALW.	A00
77	34	HW	02/20/2012	COMPAL	E4 no support WWAN SMBUS function .	Not stuff R1157 and R1158.	A00
78	35	HW	02/21/2012	COMPAL	Fix EMI issue.	Stuff CE16, CE17 & CE18.	A00
79	36	HW	02/21/2012	COMPAL	Dell E4 NB USB1457 Sansung i9100 S0 issue.	Add Q126 and remove R1613.	A00

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1	46	+1.5V_SUS /+0.75V_DDR_VT	6/25	Compal	Follow VC	Add Net SIO_SLP_S4#	X01
2	53	Selector	7/15	Compal	Module bay can not discharge	Delete connection between PR921 pin2 and PR916 pin1	X01
3	45	+5V/+3.3V	7/21	Compal	DFX concern	Change PL101 to SH00000M700 (S COIL 2.2UH 20% FDSD0630-H-2R2M=P3 8.3A) from SH00000FN0L (S COIL 3.3U 20% FDVE1040-H-3R3M=P3 11.3A) Change PL102 to SH00000OT00 (S COIL 3.3UH 20% FDSD0630-H-3R3M=P3 6.6A) from SH00000FN0L (S COIL 3.3U 20% FDVE1040-H-3R3M=P3 11.3A)	X01
4	45	+5V/+3.3V	7/21	Compal	COS concern	Change PC110 to SF000002Y00 (S_A-P_CAP 220U 6.3V M 6.3X4.2 R17M VLPS) from SGA00002M0L (S POLY C 220U 6.3V M V LESR25M PSL H1.9)	X01
5	45	+5V/+3.3V	7/26	Compal	Jitter unstable	Reserve PC120 PC121 0402 pad for improve jitter issue	X01
6	48	+1.05V_M	7/26	Compal	Jitter unstable	Reserve PC214 0402 pad for improve jitter issue	X01
7	51	VCORE_ISL95836	7/26	Compal	Fine tune Vgfx OCP and load line	Change PR711 to SD00000G780 (S RES 1/16W 422 +-1% 0402) from SD034357080 (S RES 1/16W 357 +-1% 0402) Change PR702 to SD034287180 (S RES 1/16W 2.87K +-1% 0402) from SD034255180 (S RES 1/16W 2.55K +-1% 0402) Change PR702 to SE071680J8L (S CER CAP 68P 50V J NPO 0402) from SE071330J8L (S CER CAP 33P 50V +-5% NPO 0402)	X01
8	51	VCORE_ISL95836	7/28	Compal	EMI solution	Add PL705 SM01000DJ00 (S SUPPRE_ FBMA-L11-453215-121LMA90T 1812)	X01
9	44	+DCIN	8/3	Compal	ME design change	Change PJPDC1 DCIN Cable connector to 5 pin from 7 pin	X01
10	44	+DCIN	10/17	Compal	HW add solution for S5 mode	Add PR27 SD028000080 (S RES 1/16W 0 +-5% 0402)	X02
11	52	Charger	10/25	Compal	EMI solution for reduce charger noise	Add PC1346 SE102104K8L (S CER CAP .1U 10V +-10% X7R 0402) Add PC1347 SE074102K8L (S CER CAP 1000P 50V +-10% X7R 0402) Add PL1302 SM01000DJ00 (S SUPPRE_ FBMA-L11-453215-121LMA90T 1812) Pop PC1317 SE074221K8L (S CER CAP 220P 50V K X7R 0402)	X02
12	54	PWR_PROCESSOR DECOUPLING	12/6	Compal	Change Vcore output bulk cap from 3pin to 2pin to fine tune transient_LL	Change PC1076 PC1073 PC1074 PC1075 PC1072 to SGA0000420L (S POLY C 470U 2V M D2 LESR4.5M SX H1.9) from SGA00004X0L (S POLY C 470U 2V M D2 LESR4.5M LX H1.9)	X02
13	44	+DCIN	2/15	Compal	ESD reserve PD7 for protect NB_PSID	Add PD7 SC1A204U00L (S DIO DA204U (UMD3))	

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